ARISTOTLE UNIVERSITY OF THESSALONIKI

FACULTY OF SCIENCES - SCHOOL OF PHYSICS

MSc ELECTRONIC PHYSICS – RADIOELECTROLOGY

Pixel Design for AMOLED Displays

VOSNIADIS PANAGIOTIS

Registration Number: 11244

Supervisors:

Siskos Stylianos, Professor

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The past two years I have had the chance to participate in the postgraduate program “Electronic Physics – Radioelectrology” of the Department of Physics of the Aristotle University of Thessaloniki. During these years I have broadened and deepened my knowledge in electronics and Telecommunications.

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Finally, I am especially thankful to everyone who supported me during this path.

ABSTRACT – OUTLINE

The main subject of this thesis is to develop a voltage programmable pixel circuit with a new threshold-voltage compensation technique for AMOLED displays. One of the advantages of this proposed pixel design is the simplicity of the circuit raising from the fact that requires only four TFTs and one capacitor.

Our final results for the voltage threshold variations have been confirmed by simulations. The main advantage of the proposed pixel design is that the current of the OLED is independent of the threshold voltage of the driving TFT and well controlled. Also, the threshold voltage compensation technique is implementing with a static circuit, resulting to fast response time, similar to the conventional 2T1C response time which is the fastest circuit.

The simulations for the pixel were made with *virtuoso cadence suite* and we used two TFTs models, a Low-Temperature Polycrystalline Silicon (LTPS) model and a Indium Gallium Zinc Oxide (IGZO) model.

In the first chapter the Thin-Film Transistor (TFTs) technology is presented as the most dominant technology in the area of displays. Initially an introduction to the TFTs is made, with references to the importance of the displays that use TFTs, as well as how they operate, the operation regions and the reasons why they are needed in the displays design. Subsequently, an analysis of the structure of TFTs is exhibited and the evolution of TFTs is described through a short historical review. That leads to an analysis of different kinds of the TFTs technology. Specifically, the improvement of the TFT devices characteristics, as well as the fabrication process used in the flat panel display industry. Finally, examples of Si models including amorphous silicon (a-Si), low-temperature polycrystalline silicon (LTPS) and indium gallium zinc oxide (IGZO) are listed and their advantages and disadvantages are compared to each other.

In the second chapter different types of screens like CRT-LCD-OLED are presented along with a short historical review. Additionally, a description of the basic display features of every screen is listed, as well as a comparison between them. The operation of OLED model is described and the advantages and disadvantages of LCD and OLED displays are elaborated. Furthermore, in this chapter the addressing methods in the display technology are presented. These

addressing methods have to do with the way the pixel is designed and there is a description of the three types of addressing methods: the direct method (direct), the passive matrix (PM) and the active matrix (AM). A comparison of the two basic addressing methods, the active and the passive, is also made. Finally, the architecture of the active addressing method is further described, as it is the most common method in current displays.

The third chapter is an analysis of the operation of the Organic Light Emitting Diode (OLED), which provided with a better solution to the design of the display's pixels for thinner high-performance displays and lower power consumption. Latest generation displays are developed by applying active addressing method technique (AMOLED). So, an introduction of different types of OLED is made. There is a description of the two different types of OLED, first with colored pixel and second with white pixel and colored filter above for the color production, and there is also a subsequent comparison of these two categories. Furthermore, an analysis of the two ways of pixel programming is provided, with voltage or with current, along with a comparison between the two and aiming to reveal their advantages and disadvantages. This chapter ends by describing the way that the conventional and simpler voltage programming pixel circuit 2T1C operates.

In the fourth chapter there is a step-by-step description of proposed circuit development The circuit of the project is a voltage programmed pixel (VPPC) that has some modification of the conventional voltage programmed pixel circuit (2T1C -2TFT and 1Capacitor). As indicated, the new circuit has a new threshold-voltage compensation technique applied on the conventional 2T1C. Subsequently, the operation of the circuit is thoroughly analyzed, as well as the design specifications. The time response analysis of the circuit with the parasitic capacitance and resistances is also mentioned. We analyzed the two main signals, the Vdata and the Vscan pulse, as well as the way these two pulse results to the production of the Ioled.

The fifth chapter is a presentation of the results of the simulations. First, the results are calculated for the variation of threshold-voltages, as well as the variation of carriers mobility to measure the final deviation of the current at the

driving TFT Ioled. These measurements are repeated for IGZO as well as the LTPS model, and subsequently differences between the models on the proposed pixel circuit are presented. Furthermore, a LAYOUT of the proposed pixel design is presented. Finally, there is a study on the power consumption for two cases: the full bright display and the half bright display.

In the sixth chapter, a comparison between our proposed pixel design and four other different circuits is presented, regarding the results of each of those circuits. Indications for further future projects are exposed based on our findings, mainly concerning VR displays. The final conclusions are presented in the end of this chapter.

GREEK ABSTRACT

Το θέμα της παρούσας διπλωματικής εργασίας είναι η σχεδίαση ενός προγραμματιζόμενου κυκλώματος pixel με τάση για Active Matrix Organic Light Emitting Diode (AMOLED) οθόνη. Ειδικότερα, χρησιμοποιήθηκε μια νέα τεχνική σχεδίασης για την αναίρεση των επιδράσεων της μεταβολής της τάσης κατωφλίου. Το προτεινόμενο κύκλωμα είναι μια παραλλαγή του συμβατικού κυκλώματος 2T1C (2 τρανζίστορ – 1 πυκνωτής) και ένα βασικό του πλεονέκτημα είναι ότι αποτελείται από τέσσερα τρανζίστορ και έναν πυκνωτή, κάτι που το καθιστά ιδιαίτερα απλό στη σχεδίασή του.

Τα τελικά αποτελέσματα για τη μεταβολή της τάσης κατωφλίου επιβεβαιώθηκαν με προσομοιώσεις. Το κύριο πλεονέκτημα του προτεινόμενου σχεδιασμού pixel είναι ότι το ρεύμα του OLED είναι ανεξάρτητο από την τάση κατωφλίου του TFT και είναι καλά ελεγχόμενο. Επίσης, η τεχνική αναίρεσης της τάσης κατωφλίου εφαρμόζεται με ένα στατικό κύκλωμα, με αποτέλεσμα έναν ιδιαίτερα γρήγορο χρόνο απόκρισης, παρόμοιο με το χρόνο απόκρισης του συμβατικού pixel 2T1C που είναι το ταχύτερο κύκλωμα.

Στο πρώτο κεφάλαιο της εργασίας παρουσιάζεται η τεχνολογία των τρανζίστορ λεπτού υμενίου (Thin Films Transistors - TFTs) καθώς η τεχνολογία αυτή αποτελεί την κυρίαρχη τεχνολογία στον τομέα των οθονών. Αρχικά, γίνεται μια εισαγωγή στα TFT, με αναφορές στην σπουδαιότητα χρήσης τους σε οθόνες, τον τρόπο και τις περιοχές λειτουργίας τους, καθώς επίσης και στις διαφορές τους με τα Metal Oxide Semiconductor Field-effect Transistor (MOSFET). Αναφέρονται οι λόγοι για τους οποίους τα TFT είναι απαραίτητα στο σχεδιασμό οθονών, αναλύεται η δομή τους, ενώ περιγράφεται μέσω μιας σύντομης ιστορικής ανασκόπησης η εξέλιξή τους και αναπτύσσονται τα διαφορετικά είδη τεχνολογίας TFT. Συγκεκριμένα αναλύεται η βελτίωση των χαρακτηριστικών των TFT, καθώς και η διαδικασία κατασκευής που χρησιμοποιείται στη βιομηχανία επίπεδων οθονών. Τέλος, παρατίθενται μοντέλα πυριτίου, όπως το άμορφο πυρίτιο (a-Si), το πολυκρυσταλλικό πυρίτιο (poly-Si), το οξείδιο ψευδαργύρου ινδίου γαλλίου (indium gallium zinc oxide -IGZO) και συγκρίνονται τα πλεονεκτήματα και τα μειονεκτήματά τους.

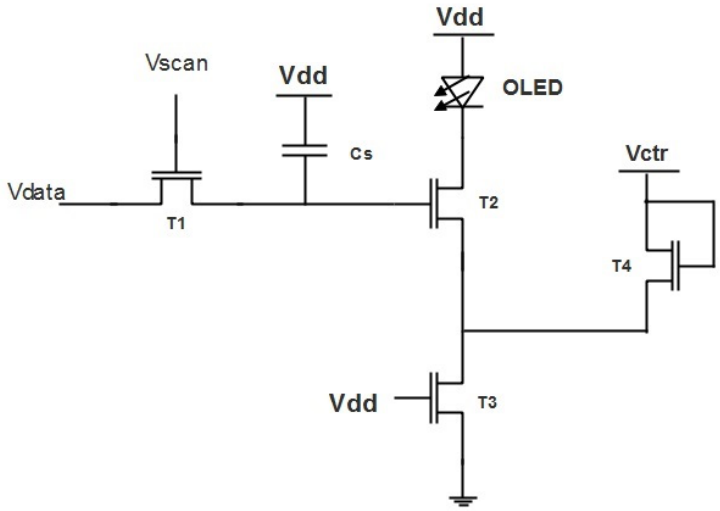
Στο δεύτερο κεφάλαιο παρουσιάζονται διάφοροι τύποι οθονών όπως οι CRT (Cathode Ray Tube) – LCD (Liquid Crystal Display) - OLED (Organic Light Emitting Diode), με μια σύντομη ιστορική ανασκόπησή τους. Συγκεκριμένα, περιγράφονται τα βασικά χαρακτηριστικά προβολής κάθε οθόνης και συγκρίνονται μεταξύ τους. Ειδικότερα, παρουσιάζεται η λειτουργία του μοντέλου OLED που χρησιμοποιείται για τις προσομοιώσεις και αναπτύσσονται τα πλεονεκτήματα και τα μειονεκτήματα των οθονών LCD και OLED.

Επιπλέον, σε αυτό το κεφάλαιο παρουσιάζονται οι μέθοδοι διευθυνσιοδότησης για τις οθόνες. Οι μέθοδοι αυτές έχουν να κάνουν με τον τρόπο επικοινωνίας του pixel με τον επεξεργαστή και είναι: η απευθείας (Direct) , η παθητική (Passive) και η ενεργή (Active) μέθοδος. Στη συνέχεια συγκρίνονται οι δύο βασικές μέθοδοι διευθυνσιοδότησης, η ενεργή και η παθητική. Καθώς η ενεργή μέθοδος διευθυνσιοδότησης εμφανίζει τα περισσότερα πλεονεκτήματα στις σύγχρονες οθόνες, περιγράφεται αναλυτικότερα η αρχιτεκτονική της.

Στο τρίτο κεφάλαιο αναλύεται η λειτουργία του OLED pixel το οποίο παρέχει μια καλύτερη λύση στο σχεδιασμό των εικονοστοιχείων για λεπτότερες οθόνες υψηλής απόδοσης και μικρότερης κατανάλωσης. Οι τελευταίας γενιάς οθόνες δημιουργούνται με εφαρμογή της ενεργής μεθόδου διευθυνσιοδότησης (AMOLED). Περιγράφονται και συγκρίνονται δύο διαφορετικοί τρόποι παραγωγής χρωμάτων σε OLED οθόνες, με έγχρωμα sub-pixel ή με λευκά sub-pixel και έγχρωμα φίλτρα τοποθετημένα στο επάνω μέρος τους. Επιπλέον, αναλύεται ο τρόπος προγραμματισμού των εικονοστοιχείων, με τάση ή με ρεύμα και συγκρίνονται οι δυο αυτοί τρόποι ώστε να διευκρινιστούν τα πλεονεκτήματα και τα μειονεκτήματά της κάθε σχεδίασης.

Στο τέλος του κεφαλαίου αυτού περιγράφεται η λειτουργία του συμβατικού και πιο απλού κυκλώματος 2T1C και η διαδικασία αναίρεσης της μεταβολής της τάσης κατωφλίου.

Στο τέταρτο κεφάλαιο περιγράφεται βήμα προς βήμα η σχεδίαση του προτεινόμενου κυκλώματος. Πρόκειται για ένα προγραμματιζόμενο κύκλωμα pixel με τάση για Voltage Programmed Pixel Circuit (VPPC) το οποίο έχει κάποιες τροποποιήσεις σε σχέση με το συμβατικό προγραμματιζόμενο με τάση κύκλωμα (2T1C -2 TFT και 1 Capacitor), όπως φαίνεται στο παρακάτω σχήμα.



Το pixel σχεδιάστηκε με τεχνολογία TFT για IGZO και LTPS μοντέλα. Το νέο κύκλωμα χρησιμοποιεί μια νέα τεχνική σχεδίασης για την αναίρεση των επιδράσεων της μεταβολής της τάσης κατωφλίου. Αναλύεται διεξοδικά η λειτουργία του κυκλώματος καθώς και οι προδιαγραφές σχεδίασής του. Λαμβάνοντας υπόψη ότι πρόκειται για μια μικρή οθόνη (5.2”), το pixel θα πρέπει να σχεδιαστεί κάτω από μια αρκετά περιορισμένη περιοχή (pixel per inch- ppi) για Full HD οθόνη (1920x1080) και ο ρυθμός ανανέωσης Frame rate να είναι αρκετά υψηλός, δηλαδή 90Hz. Για το λόγο αυτό επιλέχθηκε το ελάχιστο πλάτος των TFT της προτεινόμενης τοπολογίας να είναι 2μm και το μήκος των τρανζίστορ να κυμαίνεται από 2 έως 10μm. Η τάση τροφοδοσίας του pixel για το IGZO μοντέλο είναι στα 10V, ενώ για το LTPS μοντέλο είναι στα 6V αντίστοιχα. Μετά από υπολογισμούς για την ελάχιστη επιτρεπτή χωρητικότητα του πυκνωτή αποθήκευσης C_s, ο πυκνωτής πρέπει να είναι 100fF. Η τάση Vctr επιλέχτηκε να είναι μια σταθερή τάση στα 3V ενώ ο παλμός V_{scan} είναι ρυθμισμένος στα V_{scan}=12V, ανεξάρτητα από το μοντέλο που γίνονται οι προσομοιώσεις. Η τιμή του Vdata στο IGZO μοντέλο έχει ένα εύρος τιμών από 1 έως 9V, ενώ για το LTPS μοντέλο από 2 έως 4V αντίστοιχα.

Η θεωρητική ανάλυση του προτεινόμενου pixel επιβεβαιώνεται στη συνέχεια με προσομοιώσεις, χρησιμοποιώντας τη σουίτα *virtuoso* της εταιρίας *cadence*. Οι αναλύσεις των προσομοιώσεων αφορούν τη μεταβολή της τάσης

κατωφλίου (Vt) και τη μεταβολή της ευκινησίας φορέων (MU0) για τη μέτρηση της τελικής απόκλισης του ρεύματος Ioled από το TFT οδήγησης. Οι μετρήσεις αυτές γίνονται αρχικά για το IGZO μοντέλο και στη συνέχεια για το LTPS μοντέλο. Στη συνέχεια, στο προτεινόμενο κύκλωμα pixel και για ακριβώς τις ίδιες διαστάσεις των TFT, παρουσιάζονται οι διαφορές ανάμεσα στα δύο αυτά μοντέλα.

Οι αναλύσεις των προσομοιώσεων έδειξαν εντυπωσιακή μείωση του σφάλματος στο ρεύμα εξόδου (I_{OLED}) στην περίπτωση του IGZO μοντέλου, καθώς επίσης και ότι το ρεύμα εξόδου, για διαφορετικές τάσεις κατωφλίου, είναι ανεξάρτητο από την τάση κατωφλίου (Vt), όπως προκύπτει από τον τύπο στον οποίο καταλήξαμε: $I_{OLED} = \frac{W}{2L}\mu C_{OX}(V_{DATA} - V_{CTR})^2$. Η μέγιστη τιμή του Ioled ρεύματος επιλέξαμε να είναι 2.4 μA και στα δύο μοντέλα IGZO και LTPS, σε όλες τις προσομοιώσεις.

Στην συνέχεια περιγράφεται το layout του προτεινόμενου pixel για το οποίο χρησιμοποιήθηκε το περιβάλλον layout XL από τη σουίτα του virtuoso cadence. Δυσκολότερο μέρος του σχεδιασμού αποτελούσε η εξαιρετικά μικρή περιοχή του pixel, λόγω των προδιαγραφών της οθόνης Full HD. Έτσι, η περιοχή του κάθε sub-pixel όφειλε να είναι 60x20 um^2 και το Aperture ratio ήταν 40%. Αυτό συνεπώς σήμαινε ότι η διαθέσιμη περιοχή για το κύκλωμα ήταν μόνο 36x20um^2.

Τα υλικά που χρησιμοποιήθηκαν για τη διάταξη των εικονοστοιχείων ήταν δύο είδη μετάλλου (MET1 & MET2) και ένα πολυ-πυριτίου (POLY1). Επιπλέον, κάτι στο οποίο έπρεπε να δοθεί ιδιαίτερη έμφαση, κατά τη σχεδίαση του layout, ήταν τα τρανζίστορ T2 και T4 να είναι το δυνατότερο πιο κοντά το ένα στο άλλο, ώστε να έχουν ακριβώς την ίδια τάση κατωφλίου. Με τον τρόπο αυτό, γίνεται σωστά η αναίρεση των μεταβολών της τάσης κατωφλίου (Vt).

Στη συνέχεια, υπολογίστηκε η κατανάλωση για τις εξής δύο περιπτώσεις: την πλήρη φωτεινότητα και τη μισή φωτεινότητα στην οθόνη. Στην περίπτωση της πλήρους φωτεινότητας, η κατανάλωση στο μοντέλο IGZO είναι 72uW ενώ για το μοντέλο LTPS είναι 43,2uW. Αυτό σημαίνει ότι υπάρχει εξοικονόμηση ενέργειας της τάξης του 66%. Στη δεύτερη περίπτωση, της μισής φωτεινότητας, η συνολική κατανάλωση παραμένει μικρότερη στο μοντέλο LTPS. Για την ακρίβεια, είναι 38uW για το μοντέλο IGZO και 22uW για το μοντέλο LTPS.

Συνεπώς, υπάρχει εξοικονόμηση ενέργειας ύψους 75%. Αυτό οφείλεται στο γεγονός ότι με το μοντέλο LTPS η τάση τροφοδοσίας είναι αρκετά μικρότερη και επίσης το εύρος των τιμών της τάσης δεδομένων (Vdata) είναι αρκετά μικρότερο από το μοντέλο IGZO.

Η εργασία ολοκληρώνεται επισημαίνοντας κάποιες διαφοροποιήσεις ώστε να γίνει εφικτή η χρήση του pixel σε virtual reality (VR) οθόνες, που θεωρούνται οι πλέον υψηλής τεχνολογίας συσκευές.

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CHAPTER ONE:

Thin-Film Transistors (TFT)

1.1 Introduction

Nowadays, Thin-Film Transistor (TFTs) technology is dominant in the area of displays. It is used to fabricate small watch screens under 1 inch to computer monitors and television screens for several inches. The displays that use TFTs, replaced the Cathode Ray Tube screens (CRTs) both because of the large volume of the last ones (need a cannon for emitting electrons) and secondly because TFTs displays possess superior features, such as sharpness, resolution, frame rate, response time, contrast ratio, viewing angle [1].

A display screen made with Thin-Film Transistor (TFT) technology, having a transistor at each pixel, means that the current, which triggers pixel illumination, can be smaller and therefore can be switched on and off more quickly.

The development of TFTs made possible the creation both of flexible screens and transparent screens. In these two areas is focused the most recent research. Furthermore, semiconductor materials enabling faster TFTs, such as low- temperature polycrystalline silicon (LTPS) or transparent semiconducting oxides (TSOs), hold the promise of expanding TFT application to gate and data drivers or even full systems-on-panel, for increased reliability and lower production costs.

1.2 Structure of TFTs

A TFT is a field-effect transistor (FET) contains three terminals (gate, source, and drain) and it includes semiconductive, dielectric, and conductive layers. The semiconductor is located between source and the drain electrodes and the dielectric is placed between the gate electrode and the semiconductor. This device can control the current between drain and source (I_{DS}) by varying the potential between gate and source (V_{GS}). It also produces free charge accumulation at the dielectric and semiconductor interface [2].

In TFTs the main emphasis is on large area and low temperature processing, while metal oxide semiconductor field-effect transistors (MOSFETs) are basically concentrated in high performance, with considerably larger processing temperature.

As it is shown in fig. 1.1, MOSFETs use a silicon wafer, acting as substrate and semiconductor, while, TFTs use an insulator substrate, such as glass, that is not an active element for device operation. Furthermore, MOSFETs and TFTs have different operation mode.

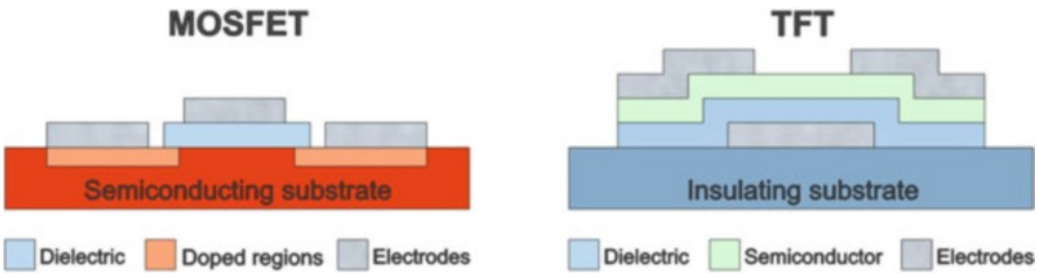


Fig. 1.1: Comparison of typical structures of MOSFETs and TFTs

The former is based on inversion, while the latter relies on accumulation. In fig. 1.2 is shown the four TFT structures according on the position of the layers. They can either be staggered or coplanar (whether drain/source and gate are on opposite or on the same side regarding the semiconductor) and, inside them, top or bottom gate (according to the location of gate) [3].

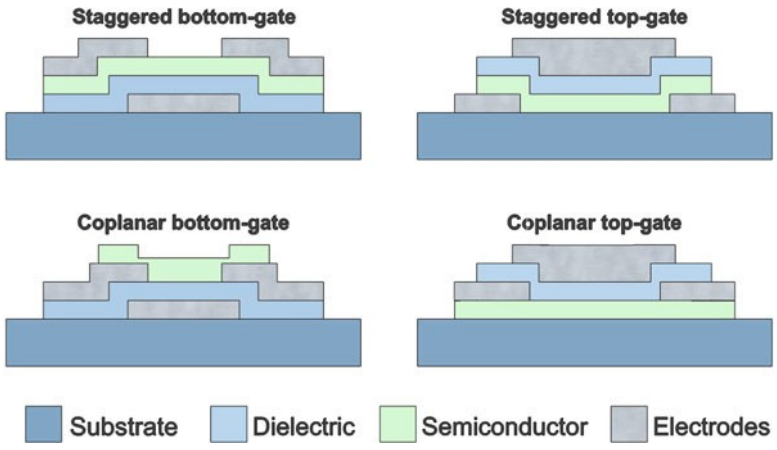


Fig. 1.2: The most typical TFT structures depending on the positioning of layers

Each of these four structures has advantages and negatives and in terms of fabrication the choice for one of these structures depends on the deposition processes and/or post-processing temperatures or number of lithographic masks

involved. For example, staggered bottom-gate structures are typically used when the dielectric layer requires high temperature, while coplanar top-gate ones are common for high temperature semiconductors, such as poly-Si [4].

Regarding operation and considering n-type TFTs, these can be designated by enhancement or depletion mode depending if threshold voltage (V_T) is positive or negative. An increase in quality mode is typically preferable because a gate voltage is not necessary to turn off the device (to achieve its Off-state) [5].

1.3 Operation of TFTs

Below will be describe the operation of TFTs, which is similar to that of the MOSFETs. Specifically, it will be examined the different cases of TFTs operation depending on the voltage existing at the gate-source V_{GS}.

As it is shown in fig 1.3, the transistor's *Cut-Off Region* specified on gate voltage, much lower than the threshold voltage of the transistor. Therefore, the condition to operate an n-type transistor in the *Cut-Off* is: V_{GS} «V_T, where V_{GS} is the voltage between the gate potential and the corresponding source and V_{TH} is the threshold voltage of the transistor. In this region, the drain currents derived from leakage currents mechanisms.

$$I_{leak} = I_o \cdot W \cdot \left[exp\left(\frac{q \cdot BLK \cdot V_{DS}}{k \cdot T}\right) - 1\right] \cdot (X_{TFE} + X_{TE}) + I_{diode} \quad (1.1)$$

where *W*, the channel length, I_o and *BLK* constants, the product kT / q is the thermal energy of the actors and V_{DS}, the drain-source voltage. Also, X_{TFE}, is the effect of thermionic field emission of carriers through the grain boundary trap states and X_{TE}, the effect of thermal field emission of carriers through the grain boundary trap states.

In the first bracket the reduction of the potential barrier due to the influence of V_{DS} is calculated. This effect is described by the constant BLK.

Finally, the reverse biased diode current of the drain contact, I_{diode}, is given by:

$$I_{diode} = I_{oo} \cdot W \cdot exp\left(\frac{-E_B}{kT}\right)\left[1 - exp\left(\frac{-qV_{DS}}{kT}\right)\right] \quad (1.2)$$

where I_{oo} is a proportionality constant and E_B is the potential barrier of the p-n contact.

When V_{GS}>V_T, a significant density of electrons is accumulated in

dielectric/semiconductor interface and a large I_{DS} starts flowing, depending on the drain-to-source potential (V_{DS}). This state is designated by On-state and involves two main regions depending on the V_{DS} value:

- If $V_{DS} < V_{GS} - V_T$, the TFT is in linear/triode mode and I_{DS} is described by:

$$I_{DS} = C_i \mu_{FE} \frac{W}{L} [(V_{GS} - V_T)V_{DS} - \frac{1}{2}V_{DS}^2] \quad (1.3)$$

where C_i is the gate capacitance per unit area, μFE the field-effect mobility, W the channel width, and L the channel length of the device. For $V_{DS} << V_{GS} - V_T$ the quadratic term is typically neglected.

- if $V_{DS} > V_{GS} - V_T$, the device is in saturation mode. I_{DS} is independent of V_{DS} and is described by:

$$I_{DS} = \frac{1}{2} C_i \mu_{sat} \frac{W}{L} (V_{GS} - V_T)^2, \quad (1.4)$$

where μ_{sat} is the saturation mobility.

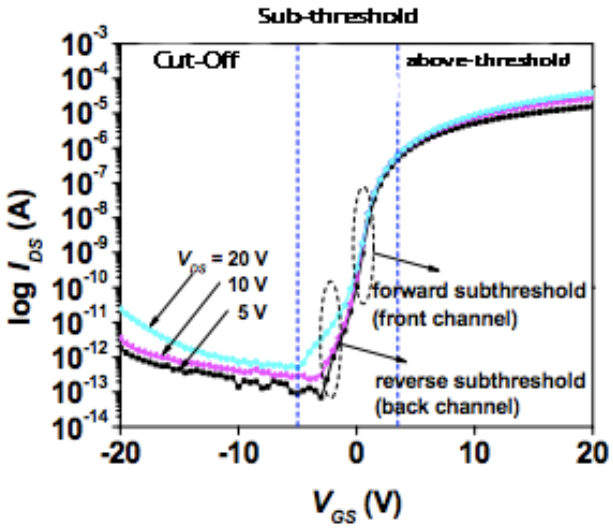


Fig. 1.3. I_{DS} as a function of V_{GS} for different values of the drain-source voltage V_{DS} = 5, 10 and 20V showing the different regions of operations

A typical characterization of TFTs involves static-current voltage measurements where output and transfer curves are obtained, as shown in fig. 1.3. While the output curve provides mostly a qualitative information regarding the effectiveness of channel pinch-off (hence saturation) and contact resistance, the transfer curve offers a more quantitative analysis.

1.4 Historical Overview

The twentieth century is characterized by the birth of electronic technology. One of the main achievement is the development of Thin-Film Transistors (TFTs), which are the main elements of the electronic flat panel displays industry. Starting with Lilienfeld in early forties, the first TFTs, as metal semiconductor field-effect transistor (MESFET) and some years later, as metal insulator semiconductor field-effect transistor (MISFET), in the coming decades have taken place very important strides in their development [6].

A main discovery for the modern electronics world was the first attempt for implementing a TFT device in 1947 by Bardeen and Brattain. It was a thin-film field effect device used a germanium film. A second main discovery, the junction field-effect transistor (JFET) was realized by Borkan and Weimer (1963) and it was based on Shockley's JFET analysis in 1952. Polycrystalline cadmium sulphide (CdS) was the material that used for the thin-film and silicon monoxide was the insulator. Source and drain contacts were placed on the opposite side of the gate. These were the first transistors that were actually fabricated, showing the switching capability of such devices and how they could be advantageous over the conventional tubes [7].

In the seventies, first, the implementation of a thin-film semiconductor instead of crystalline bulk silicon material, like Cadmium Selenide (CdSe), and second, the Active Matrix addressing method proposed by Lechner (1971) and the fact that the switch device needed in each pixel of the matrix can be materialized with the use of a TFT device, were the two very important events that changed the perspectives for TFTs. The result of the last implementation was the reduction of the fabrication cost and the decrease of the transistor size. Thin-film, formed with a-Si:H, have no grain boundaries and it was the most cost-effective technology. However, the main disadvantage of this technology was the low mobility of the carriers and the instability of the device electrical characteristics.

In the next decade the TFT technology developed rapidly. Amorphous hydrogenated silicon (a-Si:H) was introduced as a semiconductor on TFTs. Despite its low mobility when compared with the (poly) crystalline materials being studied in that period, the amorphous structure allowed for large area

fabrication, which together with the good switching capability of this technology was of great importance in defining a-Si:H TFTs as the main choice for the fabrication of active matrix liquid crystal displays (AMLCDs).

In early eighties, Lueder (1980) introduced a new approach in the TFT fabrication process. Photolithography was used instead of shadow masks that were being used since then. Their devices were optimized for liquid crystal displays applications, since the photolithography process made source-drain contacts that were self-aligned to the gate, causing the gate-source parasitic capacitance to be reduced. The compensation of the parasitic effects has improved the performance of the TFT-LCDs in the terms of the response time and the image quality. Furthermore, Depp (1981) from IBM proposed a polycrystalline silicon active layer. Pursuing greater mobility devices, TFTs based on poly-Si were introduced, allowing for high performance circuit fabrication. However, poly-Si TFTs required high temperature processes and had high fabrication cost [7].

Therefore, in the nineties, organic TFTs also appeared with a great advantage, low processing temperature, although their lack of stability and performance still remains an issue these days. Hence, for the next decades, there was still area for a new technology, combining large area uniformity, low processing temperatures, and good electrical performance.

Subsequently, the research of the TFT technology was concentrated on the improvement of the TFT devices characteristics and their fabrication process. Amorphous and polycrystalline silicon TFTs were the two main technologies that were used in the flat panel display industry. In the last decade, new TFTs technologies have been announced, like Indium gallium zinc oxide – IGZO, metamorphous silicon and organic TFTs.

1.5 Models of Si

Backplane technology describes the materials and assembly designs used for the thin film transistors which drive the main display. In other words, it is the backplane that contains an array of transistors which are responsible for turning

the individual pixels on and off, acting therefore as a determining factor when it comes to display resolution, refresh rate, and power consumption.

Examples of backplane technology include amorphous silicon (aSi), low-temperature polycrystalline silicon (LTPS) and indium gallium zinc oxide (IGZO), whilst LCD and OLED are examples of light emitting material types. Some of the different backplane technologies can be used with different display types, so IGZO can be used with either LCD or OLED displays, albeit that some backplanes are more suitable than others.

1.5.1 Amorphous silicon – a-Si

Amorphous silicon has been the go-to material for backplane technology for many years, and comes in a variety of different manufacturing methods, to improve its energy efficiency, refresh speeds, and the display's viewing angle. Today, a-Si displays is only a small percentage of the smartphone display market.

For mobile phone displays with a pixel density lower than 300 pixels per inch (PPI), this technology remains the preferable backplane of choice, mainly due to its low costs and relatively simple manufacturing process. However, when it comes to higher resolution displays and new technologies such as AMOLED, a-Si is beginning to struggle.

AMOLED puts more electrical stress on the transistors compared with LCD, and therefore favors technologies that can offer more current to each pixel. Also, AMOLED pixel transistors take up more space compared with LCDs, blocking more light emissions for AMOLED displays, making a-Si rather unsuitable. As a result, new technologies and manufacturing processes have been developed to meet the increasing demands made of display panels over recent years.

1.5.2 Low-temperature polycrystalline silicon - LTPS

Recently LTPS sits as the high-bar of backplane manufacturing, and can be spotted behind most of the high end LCD and AMOLED displays found in today's smartphones. It is based on a similar technology to a-Si, but a higher process temperature is used to manufacture LTPS, resulting in a material with improved electrical properties.

LTPS is in fact the only technology that really works for AMOLED right now, due to the higher amount of current required by this type of display technology. LTPS also has higher electron mobility, which, as the name suggests, is an indication of how quickly/easily an electron can move through the transistor, with up to 100 times greater mobility than a-Si.

For starters, this allows for much faster switching display panels. The other big benefit of this high mobility is that the transistor size can be shrunk down, while still providing the necessary power for most displays. This reduced size can either be put towards energy efficiencies and reduced power consumption, or can be used to squeeze more transistors in side by side, allow for much greater resolution displays. Both of these aspects are becoming increasingly important as smartphones begin to move beyond 1080p, meaning that LTPS is likely to remain a key technology for the foreseeable future.

The drawback of LTPS TFT comes from its increasingly complicated manufacturing process and material costs, which makes the technology more expensive to produce, especially as resolutions continue to increase. As an example, a 1080p LCD based on this technology panel costs roughly 14 percent more than a-Si TFT LCD. However, LTPS's enhanced qualities still mean that it remains the preferred technology for higher resolution displays.

1.5.3 Indium gallium zinc oxide – IGZO

Currently, a-Si and LTPS LCD displays make up the largest combined percentage of the smartphone display market. However, IGZO is anticipated as the next technology of choice for mobile displays. Sharp originally began production of its IGZO-TFT LCD panels back in 2012, and has been employing its design in smartphones, tablets and TVs since then. The company has also recent shown off examples of non-rectangular shaped displays based on IGZO. Sharp isn't the only player in this field — LG and Samsung are both interested in the technology as well.

The area where IGZO, and other technologies, have often struggled is when it comes to implementations with OLED. a-Si has proven rather unsuitable to drive OLED displays, with LTPS providing good performance, but at increasing

expense as display size and pixel densities increase. The OLED industry is on the hunt for a technology which combines the low cost and scalability of a-Si with the high performance and stability of LTPS, which is where IGZO comes in.

This technology has quite a lot of potential, especially for mobile devices. IGZO's build materials allow for a decent level of electron mobility, offering 20 to 50 times the electron mobility of amorphous silicon (a-Si), although this isn't quite as high as LTPS, which leaves you with quite a few design possibilities. IGZO displays can therefore by shrunk down to smaller transistor sizes, resulting in lower power consumption, which provides the added benefit of making the IGZO layer less visible than other types. That means you can run the display at a lower brightness to achieve the same output, reducing power consumption in the process.

One of IGZO's other benefits is that it is highly scalable, allowing for much higher resolution displays with greatly increased pixel densities. Sharp has already announced plans for panels with 600 pixels per inch. This can be accomplished more easily than with a-Si TFT types due to the smaller transistor size.

Higher electron mobility also lends itself to improved performance when it comes to refresh rate and switching pixels on and off. Sharp has developed a method of pausing pixels, allowing them to maintain their charge for longer periods of time, which again will improve battery life, as well as help create a constantly high quality image.

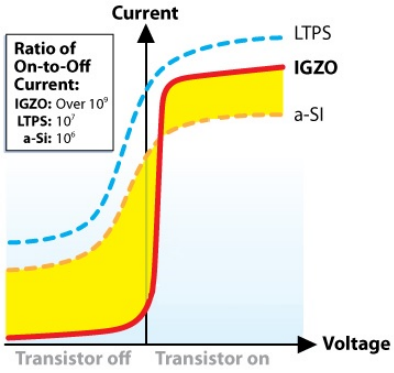


Fig. 1.4. Note the transistors at the top of each colored pixel

Smaller IGZO transistors are also touting superior noise isolation compared

to a-Si, which should result in a smoother and more sensitive user experience when used with touchscreens.

The Table 1.1, below, lists the attributes of different fabrication technologies of the pixel circuits [8].

Table 1

Comparison of TFT backplane technologies for large-area electronics

Attribute	a-Si:H	Oxide	Poly-Si	mc/nc-Si:H	Organic	IGZO
Circuit type	n-type	n-type	n-type/p-type	n-type/p-type	p-type	n-type
Mobility (cm^2/Vs)	< 1	~10	10~100	~1-10	<< 1	~10-20
Temporal stability (ΔV_T)	issue	more stable than a-Si:H	more stable than a-Si:H	more stable than a-Si:H	improving	improving
Initial uniformity	high	higher than poly-Si	low	potentially high	low	low
Manufacturability	mature	developing	developing	research	research	Research
Cost	low	low	high	low	potentially	similar to a-Si

The pixel circuits discussed above can be fabricated using different technologies, notably, poly silicon (poly-Si) and hydrogenated amorphous silicon (a-Si:H). Poly-Si technology offers high-mobility and complementary (n-type and p-type) TFTs, but has an undesirable large range of mismatched parameters over an array. This is due to the random distribution of the grain boundary in the material [9].

On the contrary, a-Si:H provides low mobility TFTs but does not provide p-type devices. Also, the threshold voltage of TFTs increases (V_T-shift) under prolonged bias stress due to the inherent instability of a-Si:H material. Besides, the technology provides good uniformity over a large area. Moreover, a-Si:H technology's industrial accessibility, by virtue of its usage in the AMLCD, provides for low-cost large-area electronics. In particular, an a-Si:H TFT backplane has the benefit of all the desirable attributes of the well-established a-Si:H technology, including low-temperature fabrication on plastic for eventual flexible electronics [10].

In addition, research is being carried out on new materials such as hydrogenated nano/micro crystalline (nc/mc) silicon, organic semiconductors and more recently, the highly promising amorphous oxide semiconductors. The nc/mc-Si:H and oxide semiconductor (e.g. indium gallium zinc oxide - IGZO) technologies provide higher temporal stability and mobility compared to the

ubiquitous a-Si:H technology [11]. However, light-induced instability can be an issue requiring special driving techniques for threshold-voltage recovery. Despite this a variety of analog and digital circuits have been demonstrated, including active matrix organic displays and imaging arrays [12].

On the other hand, an organic semiconductor has the potential for extremely low cost fabrication, including inkjet printing. However, this technology suffers from bias-induced and environment-induced instabilities and poor uniformity [13].

CHAPTER TWO:

DISPLAYS

2.1 Introduction

In the display technology, the information transmission plays the major role. In the monitor industry, the Cathode Ray Tube (CRT) has been the dominant display technology until the end of the last century. The CRT is a vacuum tube that contains one electron gun and a phosphorescent screen, and is used to display images. and it modulates, accelerates, and deflects electron beams onto the screen to create the images. The images may represent electrical waveforms (oscilloscope), pictures (television, computer monitor), or others.

One of the display technologies that deservedly replaced CRTs is the Liquid-Crystal Displays (LCDs). LCD is a flat-panel display or other electronic visual display that uses the light-modulating properties of liquid crystals. Liquid crystals do not emit light directly. The LCD monitors are eterofotous, which means that it is necessary to have a light source to the back of the screen and substantially the pixels of the liquid crystal are playing the role of switches which sometimes allow the light to pass while other times cut it. LCDs are available to display arbitrary images (as in a general-purpose computer display) or fixed images with low information content, which can be displayed or hidden. They use the same basic technology, except that arbitrary images are made up of a large number of small pixels, while other displays have larger elements. LCDs are used in a wide range of applications including computer monitors, television, phone screens and many other [14].

Another technology that dominates the display technology is the Organic Light-emitting diode (OLED). The OLED technology is used to create digital displays in devices such as televisions, computer monitors, portable systems such as mobile phones, tablets, smart watches. An OLED is a light-emitting diode (LED) in which the emissive electroluminescent layer is a film of organic compound that emits light in response to an electric current. This layer of organic semiconductor is situated between two electrodes; typically, at least one of these electrodes is transparent. A major area of research is the development of white OLED devices for use in solid-state lighting applications.

2.2 Historical Overview

In the end of the twentieth century, there was an enormous growth in small portable applications, such as mobile phones, portable computers (laptops), tablets and smart watches. All these applications required the necessary adjustment of the display technology to them, but the large volume of the CRTs was their main disadvantage and has limited their use in these kinds of devices. Thus, a new type of monitors should be found to replace the CRT.

The most satisfactory solution there were flat screens to minimize the volume occupied by the displays in the systems. It took several years of work by engineers trying to find the most appropriate type of flat screen that could replace CRT displays. In the nineties, this problem has been solved with the introduction of liquid crystal displays (Liquid Crystal Displays - LCDs) materialized with thin film silicon transistor (Thin-Film Transistors - TFTs), which was a milestone in technology semiconductor and the display industry in general. The successful development of TFT-LCD screens was not accidental. Although both liquid crystal technology (LCs), and semiconductor technologies implemented on glass substrates for Large Area Electronics (TFTs) - such as silicon thin film transistor- were well known long before the 90's, it had to be done an extended research that has led to the definition of materials and manufacturing process that could combine the two technologies and result in the completion of a TFT-LCDs screen.

The TFT-LCDs were rapidly grown and dominated the displays industry until today. They can be used in an extremely wide range of our everyday life products, like mobile phone applications, navigation systems, notebook PCs, tablets and wide screen TVs. The integration of the TFT-LCD panel peripheral driving components with low-power CMOS blocks and, therefore, the compatibility with battery operation was the main reason for the ascendance of the TFT-LCD technology in small portable applications.

The TFT-LCD monitors are eterofotous, which means that it is necessary to have a light source to the back of the screen and substantially the pixels of the liquid

crystal are playing the role of switches which sometimes allow the passage of light and other times don't. The mandatory presence of the light source resulted in the increase of power consumption and the volume of the screen. This feature limits the technical characteristics of the screen. This was the reason that there have been made attempts to find a new type of screen which would be self-luminous. In 1987, the Tank and Van Slyke, who worked at Kodak's laboratories, described a new type of LEDs, organic LEDs (Organic Light Emitting Diodes - OLEDs), so to develop a new type of screen, whose pixels based on OLED. The new screen has excellent features, with much smaller dimensions and lower power consumption. Also, the new type display is able to be constructed on flexible surfaces, such as plastic. This possibility has opened up new prospects for the development of screens. Depending on how the pixel of the display is made (LCD or OLED), there are two possible ways of the pixel driving, which will determine the way of programming: a) driving the pixel with voltage and b) driving with current. Every programming method requires a different design of the peripheral driver circuits of the matrix of the pixels of the screen.

2.3 Types of flat displays

The two main types of flat displays are the Liquid Crystal Displays (LCD) and the Organic Light Emitting Displays (OLED), as mentioned in the previous paragraph. Their basic difference has to do with the way the pixels are designed in the screens. While the LC displays are eterofotous, the OLED displays are self-luminous. Subsequently, it will be described the way the liquid crystal display as well as the LED displays are operate and design.

2.3.1 Liquid Crystal Displays – LCD

In nature the simple materials are found in three different phases: the crystal, the gas and the liquid. The particularity of the liquid crystals is that they present crystalline properties and properties of the liquid phase at the same time. The

uniqueness of these liquid crystals, is the result of their long molecules and of the oriented layout of their molecular structure. Their unique molecular structure allows the dielectric anisotropy, which are very important for constructing liquid crystal displays. Liquid crystals in the nematic phase are most commonly used in the manufacture of LCDs, because of the physical properties and wide temperature region in which exhibit stability. In the nematic phase, the molecules of the liquid crystals are oriented on average along a particular direction. By applying an electric or magnetic field, the orientation of the molecules can be altered in a controlled manner. This mechanism provides the basis for the operation of LCDs [14].

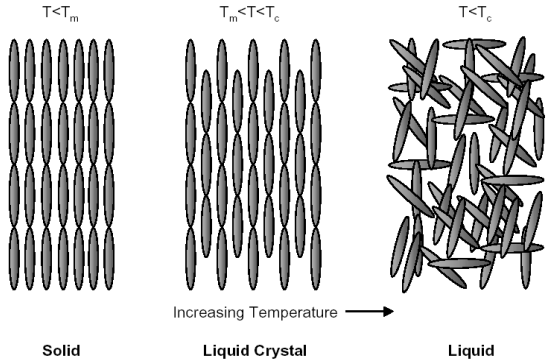


Fig. 2.1.: The three states of cholesterol benzoate, depending on temperature

In 1888, the Austrian botanist Friedrich Reinitzer conducted an experiment with a material known as benzoate cholesterol and observed changes in a solid sample of this material as he was increasing the applied temperature. Specifically, he noted that as the temperature was rising, the solid sample initially became a dull liquid and then turned into a transparent liquid. The physics professor Otto Lehmann, who had learned of the Reinitzer's discovery, conducted its own investigation to confirm that this substance appeared to have two separate melting points, Tm and Tc, as shown in fig. 2.1. He was the researcher who devised the term "liquid crystal". Then, liquid crystals are substances that presents properties of solid and liquid material, so they located in an intermediate state of matter.

In nature, liquid crystals can be found in four different phases depending on the orientation of the molecules in their molecular structure: the smectic A and C, the nematic and the cholesterol. Liquid crystals in the nematic phase are most commonly used in the manufacture of LCDs, because of the physical properties and wide temperature region in which exhibit stability. In the nematic phase, the molecules of the liquid crystals are oriented on average along a particular direction. By applying an electric or magnetic field, the orientation of the molecules can be altered in a controlled manner. This mechanism provides the basis for the operation of LCDs.

Each pixel cell of an LCD display consists of two glass substrates coated on their inner surfaces with transparent electrodes and separated by a few microns (μm) from each other. A nematic liquid crystal material fills the space between the two substrates and two polarizers are attached on both sides of the pixel with their polarization axis crossed.

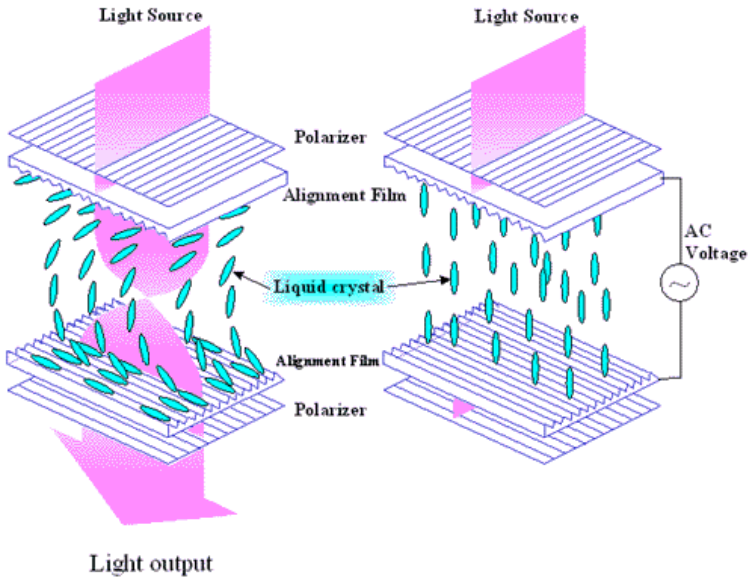


Figure 2.2.: Principle of operation of a transitional type pixel cell LCD

Externally of two glass substrates, two polarizers are attached on both sides of the pixel with their polarization axis crossed. As shown in fig. 2.2., a nematic liquid crystal material fills the space between the two substrates.

The two glass substrates, each having alignment layer, are oriented with their alignments perpendicular to each other, liquid molecule is twisted initially, as is shown in fig. 2.2. [15].

Also, the light, whose polarity is constantly changing level of polarization due to the swirling liquid crystal, is transmitted through the output polarizer. When a voltage is applied to the electrodes, the director of the molecules tends to orient themselves parallel to the applied field, since liquid crystal materials have positive dielectric anisotropy. Because, in this situation, the polarization of the light transmitted through liquid crystal is crossed to the output polarizer, the light is "cut off" and leaves the cell.

Reflective Technology has a diffuser attached to the rear polarizer. This uniformly reflects incoming light back out through the screen. Because to operate these displays require ambient light, cannot operate in an environment with dim light. These screens usually find application in pocket calculators and digital watches.

The transitional technology has a light source attached to the rear polarizer. So instead of reflecting ambient light, there is a light source within the screen. Most transitional screen technology operate with negative colors, which means that the representation of a character, the character is bright and the background is dark. The transitional technology LCDs have high image quality indoors, but is illegible in natural sunlight. This is due to the intensity of the solar light reflected on the front surface of the LCD, which is much greater than the intensity of light coming from the back of the screen. These screens have applications in medical devices, electrical measuring devices and laptops.

2.3.2 Organic Light-Emitting Display – OLED

The last decades have seen a rapid development of Organic Light Emitting Diodes, due to the characteristics they have. The great advantage of presenting the OLED displays is the fact that once flowed from electricity, glowing and emitting

light depends on the intensity of the current flowing through them. Furthermore, they present better brightness and contrast ratio compared with LCD screens [16].

Due to the fact that they do not need a light source, polarizers and diffusers, the construction of the pixel is easier and leads to lower power consumption and many other features. The structure of an OLED is shown in fig. 2.3.

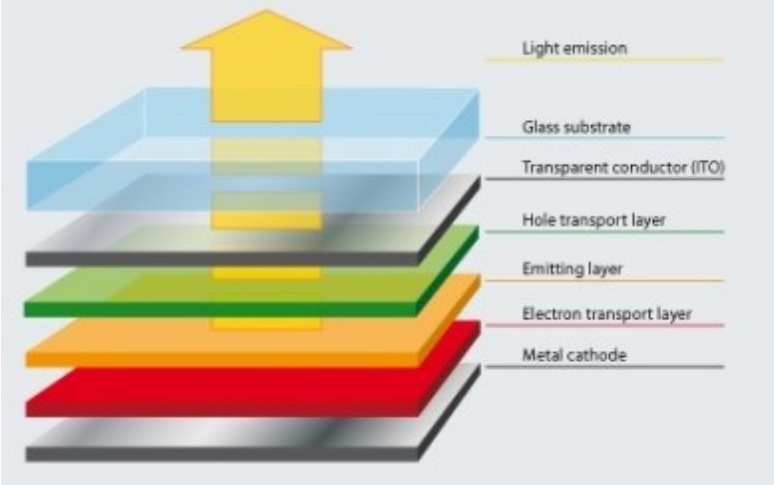


Fig. 2.3.: Structure of an Organic Light-Emitting Display - OLED

An organic light emitting diode comprises a substrate, which may be glass or other transparent material, and yet flexible, such as plastic. Then, there are two metal electrodes, the anode and the cathode, to which a voltage or current flows through. Between the two electrodes, two organic layers are placed. The first one is a conductive organic layer and the second is also an organic layer, in which, when it's applied voltage or electric current to the electrodes, diffuse carriers (electrons and holes) in this layer, which are recombine and emit light. The color of the emitted light depends on the material of the organic layer. The electrode of the anode must be a transparent material, so as to allow the generated light to emerge from the OLED. This structure has a thickness from 100 to 500 nanometers (nm). Fig 2.4 shows the characteristic curve of an OLED, and the curve showing the brightness of the produced light, compared to the applied electric current [17].

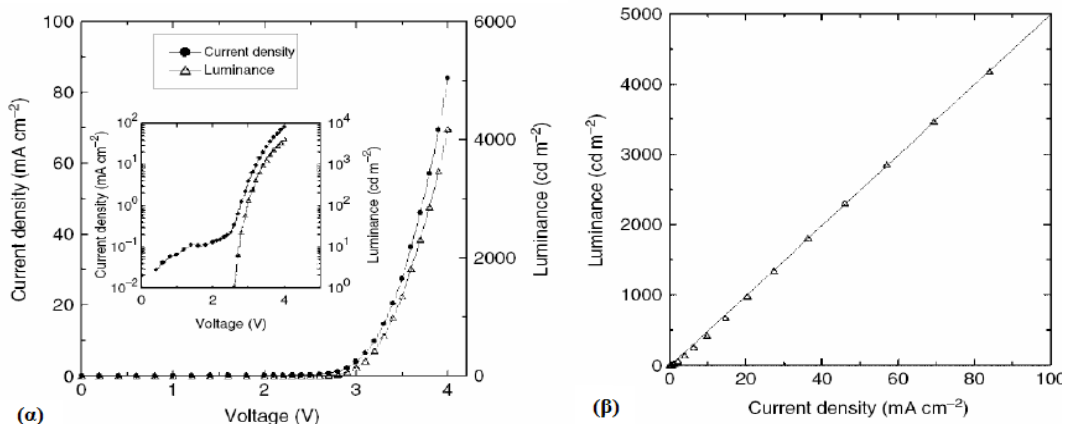


Fig 2.4 (a) Characteristic curve of a photodiode
(b) light produced Brightness as a function of applied electric current.

The characteristic curve of the photodiode resembles the characteristic of a simple diode, with the only difference that the threshold voltage of the photodiode is about 1.5 V, much higher than the threshold voltage of the single-pass. Finally, from the curve of the brightness of the produced light as a function of the applied electric current, we can see that there is a linear relationship between these two sizes.

2.3.2a OLED model

The construction and the natural operation of an OLED are the objects of extensive research. However, the characteristics of a photodiode, depend on the manufacturing process and the organic materials which they'll be used. As a result, it is difficult to find a general model that can describes the operation and the characteristics of an OLED device. Moreover, because of requirements of OLEDs market, the research has focused on how to improve the characteristics of OLED, such as lifetime and efficiency, rather than to deeply understand their function and to model them [18].

Since there is no standard model for the OLED devices, in the circuit design and pixels, LEDs are considered to be «black boxes» with empirically derived parameters. The equivalent circuit of an organic LED is shown in Fig 2.7.

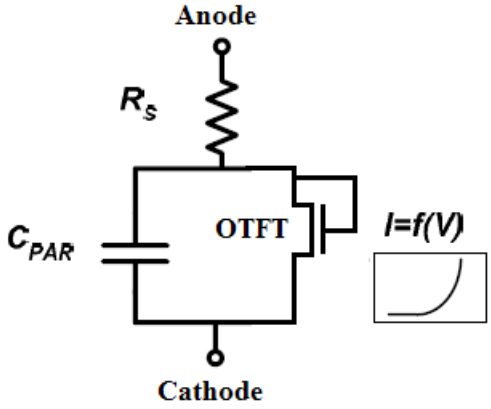


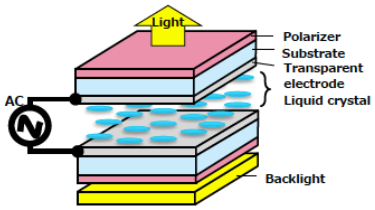
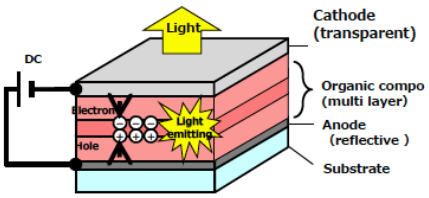
Fig. 2.7. Equivalent circuit of an organic light emitting diode.

The equivalent circuit consisted of a resistance Rs, which has a value of about 100 ohms, and a capacitor Cpar, having a value of about 25 nF / cm2, depending on the area occupied by the photodiode. Finally, in parallel with the capacitor, a TFT is connected, Diodes, whose geometrical characteristics (length and channel width) depend on the surface occupied by the photodiode, and furthermore has threshold voltage of 1.5 V. This model is generally accepted and it will be used in the simulations of OLED pixels that will follow in the next chapter. The values of the data provided are indicative and exact values depend on each case of the organic materials that will be used and the manufacturing process.

2.3.3 Comparison of the displays features

In the table, below, is summarized some of the main characteristics and differences of LCD and OLED diplays respectively. Firstly, as is shown there are differences in their structure, as for example the absence of backlight in OLED displays. Also, LCD needs AC voltage while OLED needs DC. Furthermore, the substrate of LCDs is mainly constructed by glass, while in OLED is by glass and film. As for other features of the displays, as is shown, there are differences in power consumption, flexibility and cost.

Table 2: LCD vs OLED

	LCD	OLED
Structure		
Substrate	Glass	Glass & Film
Consumption	High	Low
Design "Flexible"	Poor	Excellent
Cost	Low	Fair

2.4 Addressing Methods of Flat Display

The addressing methods in the display technology have to do with the way the pixel is designed. There are three different addressing methods: the direct method (direct), the passive matrix (PM) and the active matrix (AM). Depending on the information content that the display manages, the addressing method that will be used, can be selected. The choice of the method that will be used is a very important issue, because the peripheral driving circuits of the pixel array depends on this choice.

2.4.1 Direct addressing method

The direct addressing method, which was the first used addressing method, can be used when the content of the managed information is very small, as in the

case of the simple alphanumerical displays, such as calculators and watches. According to this method, its segment is directly connected and controlled individually by the peripheral electronics. The segments are arranged in such way so that they can produce the desired icon [19].

In the direct method, the smallest controllable component for the image production is called segment instead of pixel, which will be used in the two other addressing methods.

2.4.2 Passive matrix addressing method

The passive matrix addressing method (PM) is used in larger information applications and is a method for reducing the number of input / output lines that is required.

As it is shown in fig. 2.8, PMOLEDs have strips of cathode, organic layers and strips of anode. The anode strips are arranged perpendicular to the cathode strips. The intersections of the cathode and anode make up the pixels where light is emitted. External circuitry applies current to selected strips of anode and cathode, determining which pixels get turned on and which pixels remain off. Again, the brightness of each pixel is proportional to the amount of applied current.

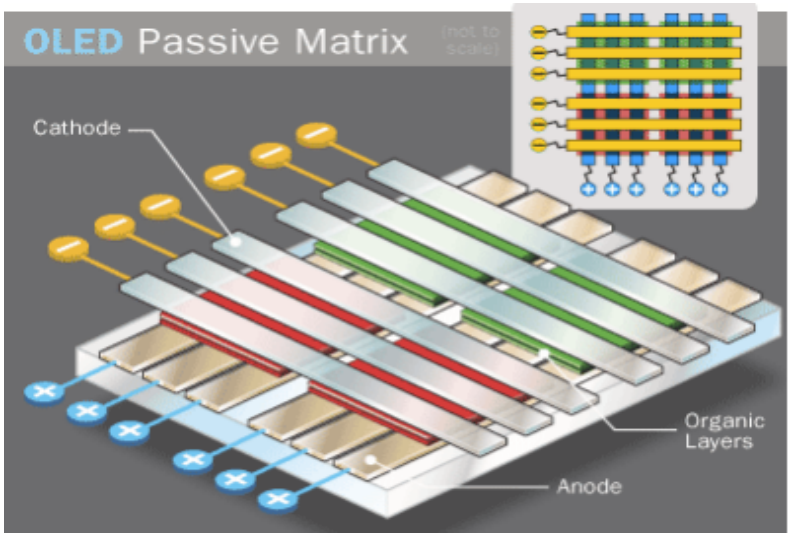


Fig. 2.8. Configuration of the passive matrix addressing method

The passive matrix OLEDs are easy to construct, but they consume more power than other types of OLED, mainly due to the power needed for the external circuitry. PMOLEDs are most efficient for text and icons and are best suited for small screens (2- to 3-inch diagonal) such as screens of cell phones, of PDAs and of MP3 players. Even with the external circuitry, passive matrix OLEDs consume less battery power than the LCDs that currently power these devices. [20]

Furthermore, the disadvantages of the passive matrix method are the low multiplexing capability and the crosstalk effect between the pixels. Crosstalk effect is caused because all the row-pixels are electrically related and a small dc voltage can be added to the pixel voltage from its neighbor pixels. The results of the crosstalk are the poor contrast ratio and the small active region of operation for the displays.

2.4.3 Active Matrix addressing method

The Active Matrix (AM) addressing method overcomes the multiplexing limitation of the PM method and the crosstalk effect. This can be achieved by incorporating a nonlinear control element, like a switch, in the cross point of the row and column lines (in series connection) of each pixel. The use of a switch will provide a 100 % duty ratio for the pixel by using the charge stored at the pixel during the row addressing time [21].

In Active Matrix, the pixels of the display panel are arranged in x-y axes. Each pixel incorporated into a nonlinear control element (TFT), which functions as an analogue switch and controls the voltage stored in the capacitor of the liquid crystal. The gate pulse of the selected row will turn “ON” the switch TFT of each pixel and simultaneously, the storage capacitor will be charged with the data voltage provided from the column driver. After the row time, the switch TFT will turn “OFF” as soon as the negative edge of the row pulse is delivered and the pixel will be isolated from all its neighbor pixels until the next frame time. This process addressing looks like giving the coordinates (x, y) of the pixel on the panel we want to program so each pixel is independent of the other.

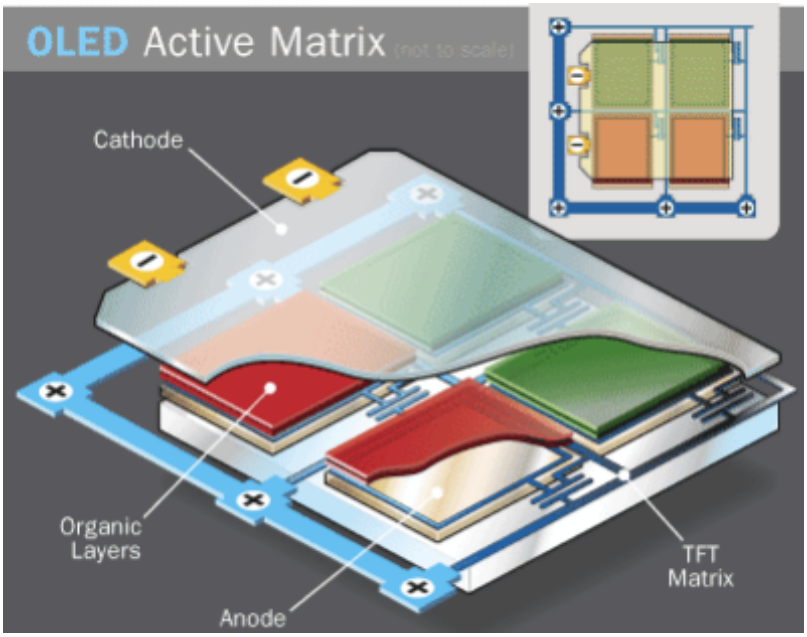


Fig. 2.9. Configuration of the active matrix addressing method.

Fig. 2.9. shows in Active Matrix OLEDs have full layers of cathode, organic molecules and anode, but the anode layer overlays a thin film transistor (TFT) array that forms a matrix. The TFT array itself is the circuitry that determines which pixels get turned on to form an image.

AMOLEDs consume less power than PMOLEDs because the TFT array requires less power than external circuitry, so they are efficient for large displays. AMOLEDs also have faster refresh rates suitable for video. The best uses for AMOLEDs are computer monitors, large-screen TVs and electronic signs or billboards.

2.5 The Peripheral Circuit Driving Architecture of Active Matrix Display

In Active Matrix applications, the pixels of the display are programmed by the line-at-a-time method. During one frame, all the Gate Bus rows progressively

scanned with a pulse value $V_{gate,\ sel}$, while at the same time the Data Bus shows the respective data voltage, V_{data}. Suppose that appears on the screen the new image frame. Then, in the first Gate Bus line, $V_{gate,sel}$ voltage will be applied, which will force TFT switches of the first line turn to the "ON" state. In all Gate Buses of the remaining rows, the voltage $V_{g,non\text{-}sel}$ is applied, causing switches of the pixel to be "OFF" state. At the same time, the necessary voltage V_{data} applied to the Data Buses. Since, only the pixels of the first row is "ON", only these will be programmed. As soon as even the last pixel of the first row has been programmed, voltage $V_{g,non\text{-}sel}$ applied to the Gate bus and all its pixels are closing.

2.5.1 Architecture of Active Matrix Display

The fig. 2.10, below, shows the Architecture of an Active Matrix screen including the pixels array and the peripheral control and driving circuits of the matrix.

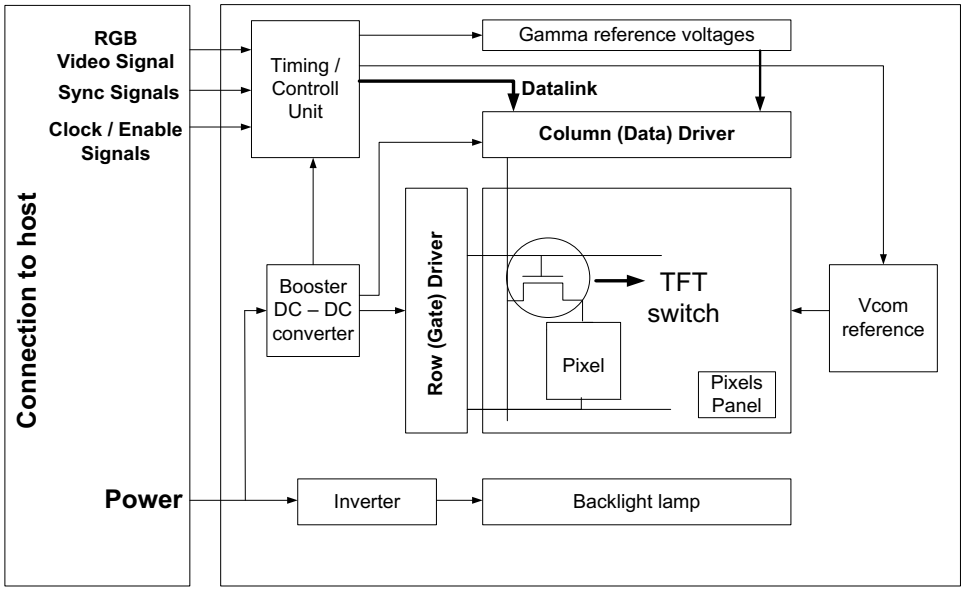


Fig. 2.10. Architecture of Active Matrix Display

The difference between AMLCD and AMOLED display is the absence of the light source (inverter + backlight lamp) on the back of the pixels matrix. The other circuits are similar. Two very important block circuits are those of the timing and control (timing / control unit) and power (booster and DC - DC converter). The timing and control block is basically that, which receives, as input, the video signals (RGB) and translates them into digital signals which are distributed to the other block.

Furthermore, it generates the signals for the clocks of the other block, as well as the synchronization signals of the block together. We can say that the control and timing unit is the "heart" of an Active Matrix screen.

The digital signals of the image are distributed at the column or data driving circuits (column / driver data), and synchronization signals are distributed to row driving circuits or gate (row / driver gate). The row / column peripheral circuits will be described in more detail in the following paragraphs [22].

2.5.2 Gate / Row Driver Circuits

The row driver block function is the production of line selection signals that controls the synchronization during the programming of rows. Essentially, it produces the signals that are applied to the gates of TFT switches (that each pixel has), and determine if the switch is on "ON" or "OFF" state.

That is why they are often called block and gate drivers. The line selection voltage (V_{sel}) must be at least twice bigger than the threshold voltage of the TFT switches to ensure that the switch will operate in saturation area, while the non-selection voltage ($V_{non\text{-}sel}$) should be two times smaller than the threshold voltage so that the TFT will be in the cut-off region.

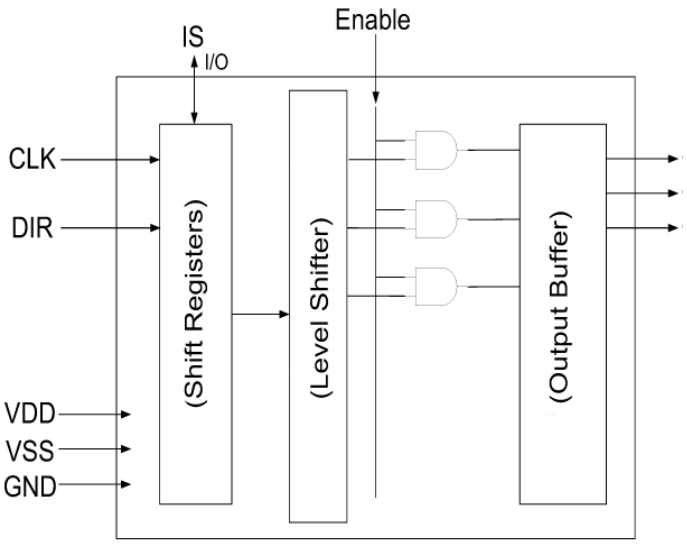


Fig. 2.11. Architecture of Row / Gate Driver Circuits.

The duration of the signal line selection pulses is from 10μm to 70μm, depending on the number of lines of the pixels matrix and the duration of the frame. These features are the design specifications of the row driver circuit [23].

2.5.3 Data/Column Driver Circuits

The column driving circuit block is more complicated than the row block. The operation of block column driver based on converting the digital image input signal (input digital video signal), into an analog data output signal (output analog data signal) which will be transferred to each pixel. That's why the column driver block often is called data driver block.

The level of the output voltage represents the gray-scale level or of the color that we want for the pixel to emit and it is transferred to the source of the pixel's TFT switch of the same row simultaneously. The brightness emitted by OLED is proportional to the current flowing through Driving TFT. This way, the transformation of V_{data} to I_{oled} determines the gray-scale.

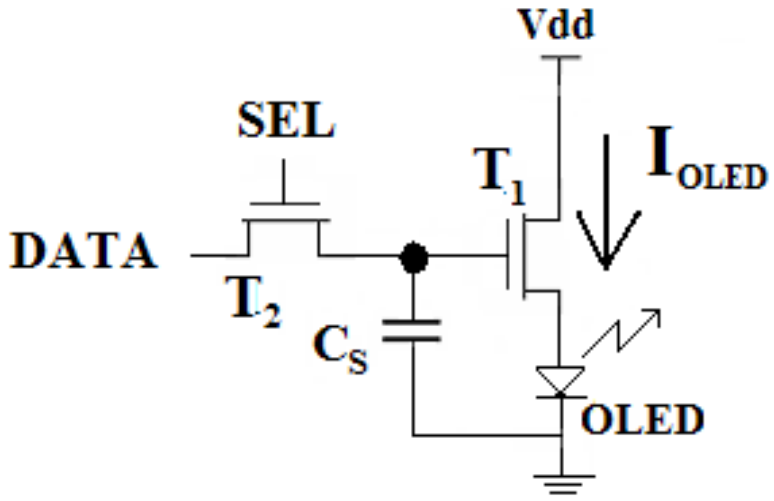


Fig. 2.12. AMOLED pixel, consisted of two TFTs and one storage capacitor Cs (2T1C)

In both case of LC and OLED pixels, in order to have proper pixels' operation and illumination, the data voltage must be at least about 2 V. This data voltage may reach up to 10 V, depending on the materials used and the number of the gray-scale that the light emitted by the pixel will have. To achieve such an output voltage, the data driving circuits need voltage supply range to 15 V. In special cases, such as large high quality screens, the voltage supply can be as high as 20 V to 25 V. Fig. 2.13 shows the architecture of the data driver block.

A block data driver consists of a bi-directional shift register, which may be implemented in the architecture of multiple successive registers, as in the case of the row driver block. Thus, we achieve scanning the screen from both sides (from right to left or vice versa).

The input start (IS) determined from which side will be the scanning. The digital signals for the three primary colors (red-green-blue) are the *latch input signals*. After the signals are recorded in the latches, they are transferred to the level shifter, to be strengthened and to acquire the necessary voltages values.

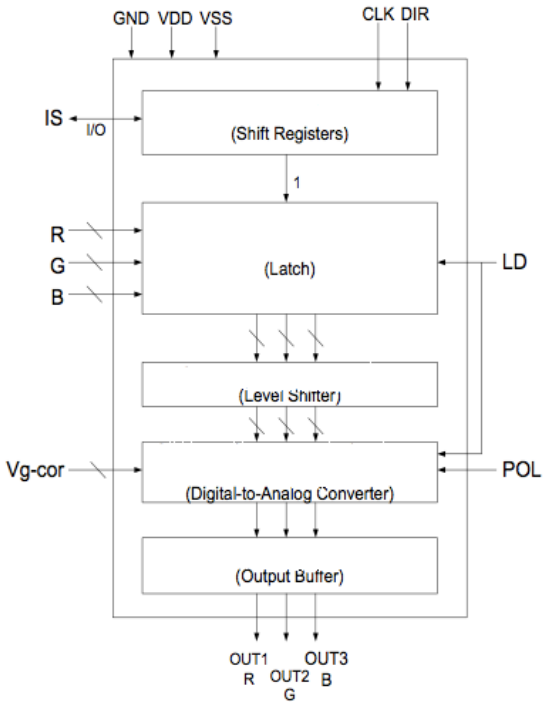


Fig 2.13. Architecture of data blocker

Depending on the number of rows and columns, a display has, the video format of the screen is characterized. The ratio of the number of display columns to the corresponding number of rows, is called aspect ratio, while the product of the number of rows and the number of columns is called the resolution of the display. For common screens the aspect ratio is 4:3, while for wide screens, the ratio is 16:9.

Finally, the introduction of new flat panel displays, like Organic Light Emitting Diode (OLED) displays, and the flexible substrate displays have created the need for new TFT technologies, compatible with the new types of flat panel displays.

CHAPTER THREE

Organic Light Emitting Diode

3.1 Introduction

The Organic Light Emitting Diodes gave a better solution for the design of the display's pixels for thinner high-performance displays, with lower power consumption. Such displays could be designed with both addressing techniques, active (AMOLED) and passive (PMOLED).

An AMOLED display consists of a certain number of pixels, which are distributed in rows and columns. The total number of pixels of the screen determines its sharpness. The dimensions of a screen is counted by the length of the diagonal, which is usually measured in inches. Also, the ratio of the number of the lines of the pixels to the corresponding number of columns, called ratio of dimensions and is defined for all screens. Formerly the ratio used to be 4:3, but the current wide screens have ratio 16:9.

The AMOLED display's Pixels are divided in two parts: The first is the OLED, which illuminate according to the current flowing and the second part is the circuit which generates the necessary current of the OLED, as shown in Fig. 3.1.

The circuit part is not transparent, while only OLED radiates. The ratio of the transparent area (OLED) to the ratio of the non-transparent surface (circuits with lines), called the aperture ratio. Finally, in each pixel there are rows of signals, which is the selection signal from the block line driver, the data signal coming from the block column drivers and the supply voltage.

As the objective of the displays is color production. With the appropriate combination of the three primary colors, Red - Green – Blue (RGB), all colors in nature can be created. There are two ways for color generation for OLED displays. First way is with color OLEDs and the other way with only white ones and color filters. Both ways have advantages and disadvantages [24].

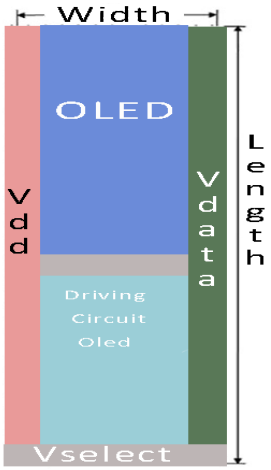
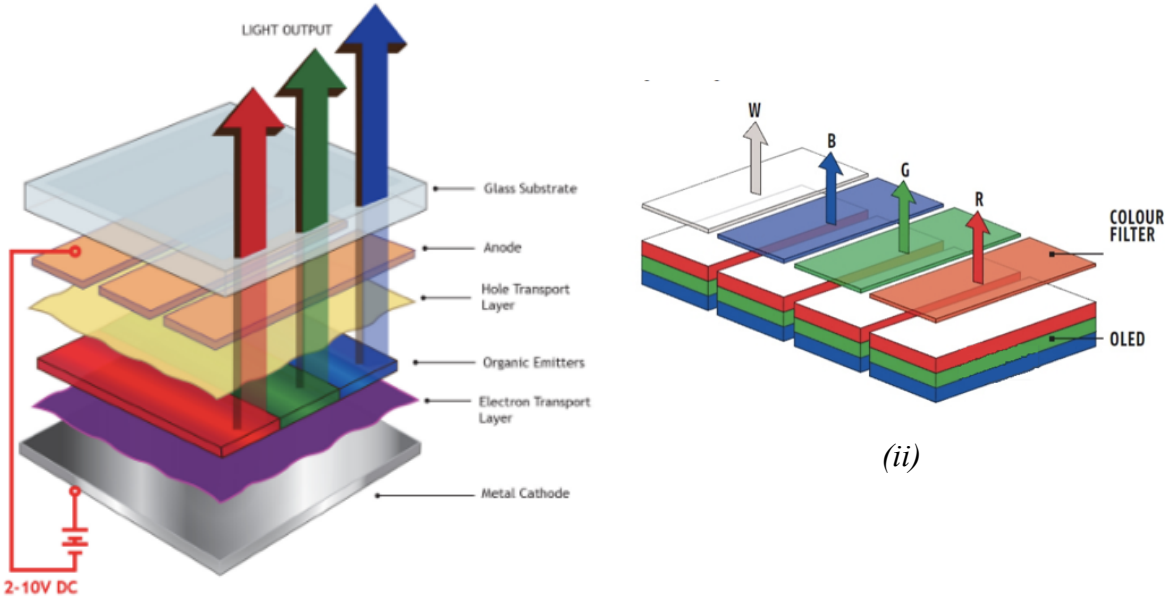


Fig. 3.1. Schematic representation of a pixel of an AMOLED display

The first way, is the method of depositing RGB emitting layers at each pixel and it is called the *Shadow Mask Patterning Method*. Since the displays produced by this method have independent emitting layers they have excellent color purity and contrast. Also , it is possible to have high luminance efficiency and low power consumption, because there are no need of RGB color filters to use.

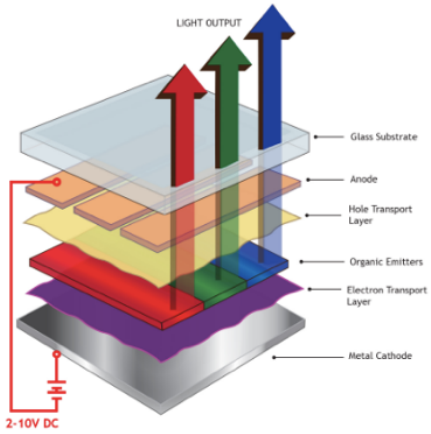
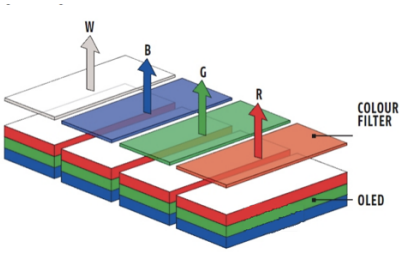


(i) *(ii)*

Fig 3.2. i) Color Oled - Shadow Mask Patterning Method, ii) Color Filter Method

Table 3.

Structure of the two different ways of color production - advantages/disadvantages

	Positives	**Negatives**
 *Color Oled - Shadow Mask Patterning Method*	• High color purity • High Contrast • Low power consumption	• High accuracy for deposition Required • Various lifetime lengths depending on each pixel
 *Color Filter Method*	• Simple production • No difference lifetime	• High energy loss • High power consumption

The second way, is the method which produce colors through the use of RGB color filter and it is called *Color Filter Method*. With this method, the OLED materials, including RGB color elements, produce white light which is then filtered to obtain the desired colors. It is not necessary to have a wide variety of OLED materials so only one kind of OLED material is used to produce white light. Some disadvantages are low color purity and contrast. Also, the filters used with the method absorb most of the light energy emitted, requiring the white light to be relatively strong. Therefore, power consumption for the displays produced by this method is higher. Both mono-color panels and full-color panels have these

characteristics. The two figures in fig. 3.2 show the structure of the two different ways of color production.

Table 3 shows the structure of the two different ways of color production, as well the advantages and the disadvantages of the two ways of color production.

In order each pixel can illuminate all colors, it is divided into three sub-pixels, each of which illuminates a base color. As the pixel has a square shape, the width of each sub-pixel is the 1/3 of its length, as it is shown in fig. 3.3. Each color is created by the light intensity produced by the OLED, which it is determined by the current flowing through it.

The circuit of the pixel can be implemented by various thin-film transistor technologies. The two main technologies used by the industry, are amorphous silicon transistors (a-Si TFTs) and polycrystalline silicon (pc - Si TFTs).

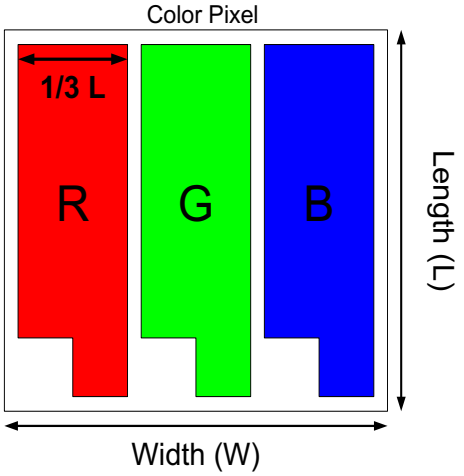


Fig. 3.3: Typical full color square pixel

Despite the stability of their characteristics, when the a-Si TFTs subjected to electrical stress (stress), then a temporary threshold voltage shift observed, due to the intrinsic properties of the amorphous material. [25]

The light emitted by the OLED, depends solely on the current that flows through. Therefore, the current must be very well controlled and stable so as to

ensure the uniformity of the screen. The current flowing through the OLED is generated by the analog circuit of the pixel. Changes in threshold voltage of the TFT transistors, regardless of technology, will cause instability in the current, resulting in the reduce of the display's performance. This means that the power output of OLED circuit must be properly designed so as its behavior not to be affected by the threshold voltage changes [1].

3.2 Programming methods

Active matrix organic light emitting (AMOLED) are considered potential future display technology, as they are thin, have a high degree of brightness, are self-emitting, have fast response time, a high contrast ratio and are flexible. The approaches for driving AMOLED pixel circuits can be divided into two kinds: the current programming method, and the voltage programming method.

3.2.1 Current Programming Method

The current programming method can be divided into current copy and current mirror, Fig 3.3. Current copy technology adjusts the control-signal and pixel structure to store sufficient voltage in the capacitor to generate the same input data current (I_{DATA}). Then, TFT switching is controlled and the I_{DATA} is copied and functions as the OLED current. Conversely, the current mirror technology with a symmetrical structure produces the driving current, which is multiple I_{DATA}. The current method can overcome variations in electrical characteristics of the TFT process, such as mobility and threshold voltage. However, these current-programmed methods require prolonged settling time at a low data current and inconvenient constant current sources that control sub micrometer ampere-level current in peripheral drivers. Thus, the current driving method is unsuitable for large-high-resolution displays.

In the current programming driving scheme, the programming current flows through a diode-connected TFT during the programming time, and the gate-source voltage of the TFT is stored in a capacitor. The current is replicated by the pixel

circuit for the OLED during the hold (frame) time. Such a driving scheme compensates for the V_T shift in the TFTs since the OLED current does not directly depend on the characteristics of the drive TFT. Generally, current-programmed pixel circuits (CPPCs) are categorized as mirrored and non-mirrored circuits. As implied by the names, in a mirrored pixel, the sampling of the programming current and the driving of the OLED are performed by a current mirror. In a non-mirrored pixel circuit, the same TFT samples the programming current and drives the OLED.

Fig. 3.4(a) shows the basic circuit diagram of a typical non-mirrored CPPC. It consists of an OLED, a storage capacitor (C_S), a drive TFT (T1), and some switch TFTs (S1 to S3). During the programming cycle, S1 and S2 are turned on and S3 is turned off. The programming current flows into the drive TFT through S1 and the gate-source voltage of T1 is stored in C_S through S2. After the programming cycle, S1 and S2 are turned off and S3 is turned on. A copy of the programming current continues to flow into the OLED, since the gate-source voltage of T1 is stored in C_S.

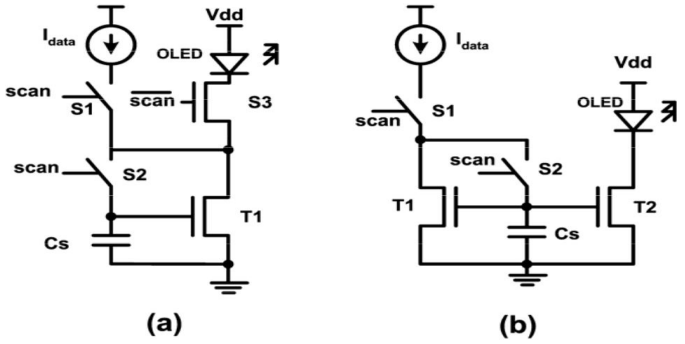


Fig. 3.4: Conceptual circuits of current programmed pixels:(a) non-mirrored, (b) mirrored.

Fig. 3.4 (b) shows the general implementation of a mirrored CPPC. Here, T1 and T2 form the current mirror, and S1 and S2 are the switches. When the pixel is programmed, S1 and S2 are turned on, allowing the current to flow into T1. If both T1 and T2 operate in the saturation region, the amount of current that passes through the OLED depends on the sizes of T1 and T2. After programming, S1 and S2 are turned off. Since the gate-source voltage of T2 is stored in C_S, the current through

T2 does not change considerably. Assuming that T1 and T2 have identical characteristics, the current through T2 is a replica of the programming current.

The OLED current in the mirrored CPPCs depends on the ratio of the size of T1 to the size of T2. Consequently, in contrast to non-mirrored pixels that always have a unity gain, it is possible to design mirrored CPPCs with various gains. Another difference in the circuit topology between mirrored and non-mirrored CPPCs is that in most of the presented non-mirrored pixels, two TFTs are in the driving path. As a result, the non-mirrored pixels require higher supply voltages, and therefore consume more power. Mirrored CPPCs have only one TFT in the driving path. However, the matching of the current mirror TFTs must be high enough to achieve a high current uniformity over the display.

3.2.2 Voltage Programming Method

The compensation principle of the voltage driving method can be sorted as self-compensation and TFT-matching. The self-compensation method stores the threshold voltage (VTH) information of driving TFT for compensation during the programming process. The TFT-matching method compensates for threshold voltage variations when driving TFTs by utilizing the neighboring TFT VTH, which is assumed to have the same electrical characteristics as the driving TFT. Additionally, the voltage driving method is appropriate with fast programming time for application to large-high-resolution displays. Table 3.2 compares current and voltage program methods.

Table 4.
Comparison between voltage programming and current programming methods.

Method	**V_{TH} Compensation**	**Charge time (low gray level)**	**Signal Source Manufacture**
Voltage Programming	Provide	Fast	Easy
Current Programming	Provide	Slow	Difficult

Regarding the programming method, the first pixel topology proposed for AMOLED displays, is consisted of two transistors and a storage capacitor Cs (2T1C), as is shown in fig. 3.5 [26].

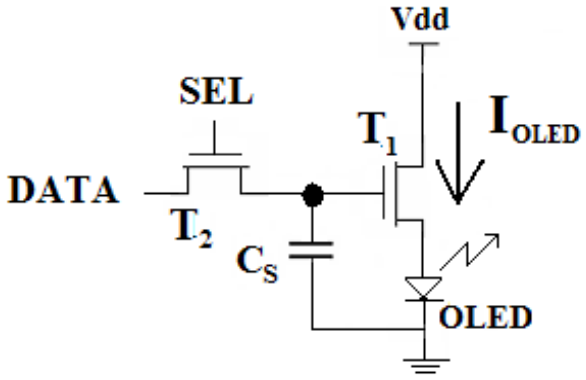


Fig. 3.5. AMOLED pixel, consisted of two TFTs and one storage capacitor Cs (2T1C)

This topology is the simplest and quickest and consists of a transistor acting as a switch (T2) and the driving transistor (T1). When the pixel is programmed, the voltage of the row selection signal (select), from the block line driving, causes T2 to switch in "ON" state and the data voltage (data) is stored in the capacitor Cs. During light emission, T2 goes to "OFF" state and the T1 produces the OLED driving current (I_{OLED}), which depends on the stored voltage of the capacitor.

The biggest problem of this topology is that the driving current of the OLED is depending by the threshold voltage of T1. This means that if in two neighbor pixels, are stored the same data voltage and normally should be glowing the same color shade, the result will be different due to different threshold voltage having their driving transistors. Thus, the performance of these pixels was limited.

3.3 Design Techniques AMOLED Pixel for Cancelling the Effect of the Variation of Threshold Voltage

In the above paragraph is presented the existing design techniques AMOLED pixels, which will produce a constant current, regardless of the threshold voltage of TFTs.

In all techniques, the undo of the changes' effects in the threshold voltage, is based on the increased data voltage during a V_{th}, the tendency in the driver transistor gate is equal to $V_{GS} = V_{data} + V_{th}$. In this case, the current that produces the driving transistor, since it works in the saturation area and without considering the kink effect, will be given by the following equality:

$$I_{DRAIN} = \frac{W}{2L}\mu C_{OX}(V_{GS} - V_{th})^2$$

$$I_{DRAIN} = \frac{W}{2L}\mu C_{OX}(V_{DATA} + V_{th} - V_{th})^2$$

$$I_{DRAIN} = \frac{W}{2L}\mu C_{OX}{V_{DATA}}^2, \quad (3.1)$$

where W and L is the width and length of the channel, respectively, with the agility of organizations and Cox is the gate oxide capacitance per unit area. Based on the relationship (3.1), the current that flows through the OLED depends only on the dimensions of the driving transistor and the data voltage and is independent of the voltage of the transistor threshold.

Under the new design technique, instead of increasing the voltage to the drive transistor gate as a threshold voltage, the voltage at the transistor source is reduced by an opposite sign threshold voltage, i.e. for the driver transistors to apply $V_G = V_{data}$ and $V_S = - V_{TH}$. The gate voltage - source (V_{GS}), defining the OLED driving current in this case would be [27]:

$$V_{GS} = V_G - V_S \quad (3.2)$$

$$V_{GS} = V_{DATA} - (-V_{TH}) \quad (3.3)$$

$$V_{GS} = V_{DATA} + V_{TH} \quad (3.4)$$

From the equation above, we find out that with the new design technique, the gate voltage - source is the required one, so that the current generated by the driving transistor will be given by formula (3.1) and therefore it is independent of the voltage of the transistor threshold. The big advantage here is that there is disengagement of the technique for cancelling the changes in the threshold voltage from the node of the transistor gate and consequently from the dissemination of data's path, as it can be implemented by a static block connected to the terminal source.

In the following chapter, we will develop the proposed pixel design, based on the above theory of cancelling the effect of the variation of threshold voltage.

CHAPTER FOUR

Pixel Design

4.1 Introduction

The new threshold-voltage compensation technique can be applied to the simple voltage programmed topology (2T1C) which is shown in fig 4.1, resulting in a new AMOLED pixel topology. The new topology is implemented with n-type TFT in IGZO and LTPS models. That's because IGZO TFT are available only in n-type and it was important to keep the same schematic in order to compare it with the LTPS. The concept behind the threshold-voltage compensation pixel's design, is shown in fig. 4.2.

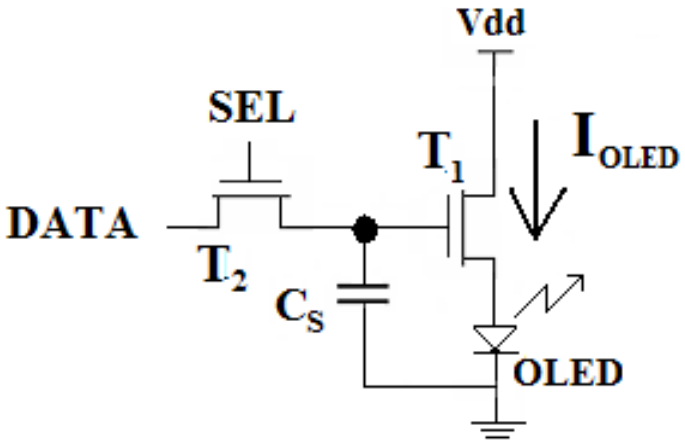


Fig 4.1: Simple voltage programmed circuit (2T1C)

As demonstrated in fig. 4.2, the new topology consists of a voltage programmed pixel circuit (VPPC). The transistor T1 functions as a switch and the transistor T2 converts voltage to current for the OLED. Since it is an n-type implementation, the OLED is connected to the power source while the threshold voltage compensation circuit is in the Drain of T2 and in VSS.

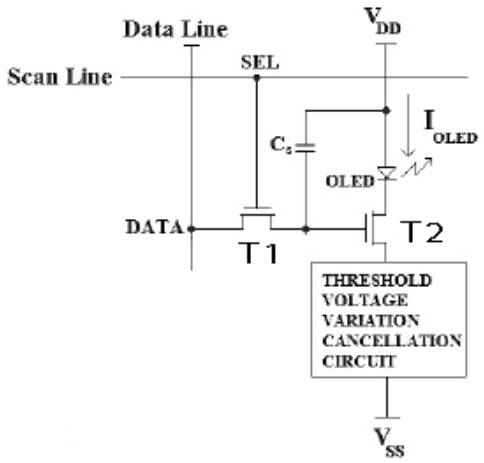


Fig 4.2: The implementation of threshold-voltage compensation technique with n-type TFT

The new pixel circuit is a voltage programming circuit or a VPPC. It is designed only with n-TFT and it contains four TFTs and a storage capacitor. To maximize the pixel stability, we chose to connect one of the two terminals of the storage capacitor with power supply instead of ground. The other terminal of the capacitor is placed at the gate of Driving TFT (T2) to storage the data voltage after the programming phase, as is shown in the schematic representation in fig 4.3.

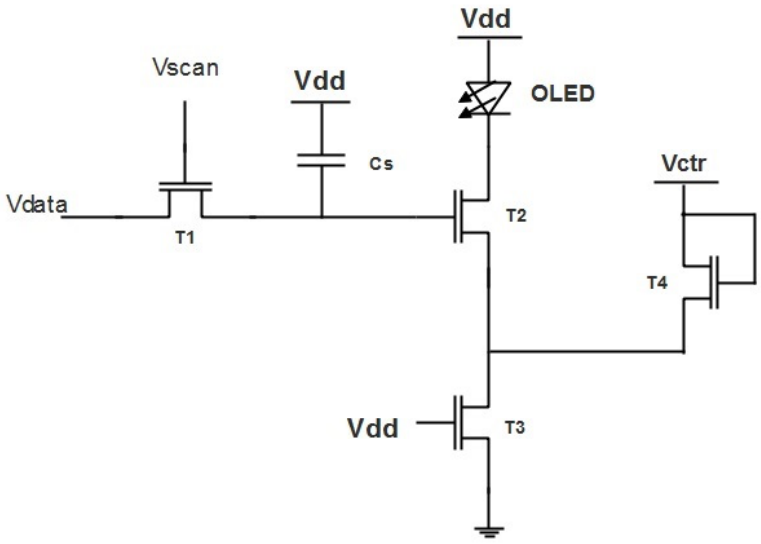


Fig. 4.3: Schematic representation of the proposed pixel circuit

The proposed pixel topology has been designed by taking into account the cutting edge technology characteristics of a Full HD screen, as they are used in mobile phone and with high Frame rate.

The theoretical analysis of the pixel will be confirmed by the simulation, using the *cadence virtuoso software*. As mentioned, the pixel will be designed under IGZO and LTPS TFTs technology. A small display will be considered, which implies that the pixel has to be designed under a limited area (high pixels per inch – PPI) to fit in a Full HD. This means that the available area is very small, so the minimum length of the TFT of the proposed pixel topology has to be kept at 2μm.

In Table 5 below, the transistors size is shown, as well as the values of power supply and the storage capacitor.

Table 5

Circuit parameters values

Element	**Value**
T1	4/2 μm
T2	10/2 μm
T3	4/2 μm
T4	2/8 μm
$C_{storage}$	100 fF
Vdd (IGZO)	10V
Vdd (LTPS)	6V
Vctr	3 V
V_{scan}	12 V

4.2 Circuit operation

In paragraph 3.3 we have already described the theory, in which the design of the pixel is based on. As mentioned before, the operation of the pixel is divided into two phases. In the first phase, the programming of the pixel takes place. During this phase the transistor T1, which operates as a switch, turns “On”, when the signal of

the Vscan goes to high level. The data voltage that is applied to the drain of transistor T1 is stored in the capacitor (Cs), which is connected in the gate of Driving TFT (T2).

During the second phase, which is called the emission phase, Vscan signal goes low and resulting in T1 switch to turn "OFF". The transistor T2, which operates in saturation region, produces the current that will drive the OLED and it is equal to:

$$I_{DRAIN} = \frac{W}{2L}\mu C_{OX}(V_{GS} - V_{TH})^2 \quad (4.1)$$

The T4 transistor is diode connected, which means that the gate and the drain of T4 are shorted. In that way the source of T4 must be the subtraction of the V_{ctr} power supply minus the threshold voltage (V_t). Thus, the source of driving TFT (T2) is V_s and is equal to V_{ctr} -V_t. For better results, it is chosen that V_{ctr} = 3Volt. Furthermore, the V_g will be V_{DATA} after the programming phase, so $V_{GS} = V_G - V_s$ and the current drain is equal to:

$$I_{DRAIN} = \frac{W}{2L}\mu C_{OX}(V_{DATA} - V_{CTR} + V_{TH} - V_{TH})^2 \quad (4.2)$$

and finally:

$$I_{DRAIN} = \frac{W}{2L}\mu C_{OX}(V_{DATA} - V_{CTR})^2 \quad (4.3)$$

In addition, T3 transistor has to operate in the linear region and acts as a resistance. There are two necessary conditions for a transistor to work in a linear region:

$$V_{GS} > V_T \quad (4.4)$$

and,

$$V_{DS} \leq V_{GS} - V_T \quad (4.5)$$

In the pixel design, in order to save space in the layout design, the gate voltage of (T3) is preferred to be equal to the power supply voltage (9V) and at the same time both necessary conditions are fulfilled (4.4 & 4.5). In this way, the current of OLED is independent of the voltage threshold of the TFTs, as well as stable and well controlled. So, the light that every pixel is emitting is exactly the same, which

is of great importance for the best operation of the display. The basic advantage of the proposed pixel topology is that the threshold-voltage compensation technique implemented with a “static” circuit.

4.3 Design specifications

The proposed voltage-programmed pixel circuit will be designed under specifications for Full HD display format dedicated to mobiles. The specifications of this application are shown in Table 6.

Table 6: Full HD specifications for a 5.2 inches for mobile.

Parameters	**Value**
Screen type	Full HD
Aspect ratio	16:9
Resolution	1920x1080
Diagonal size	5.2 inches
Pixel per Inch	~423
Brightness OLED	200 cd/cm^2
Ioled,max	2.4μA
Gray-scale	8-bit
Frame rate	90Hz
Frame Time	11,1ms
Programing Time	10μs
Pixel size	60μm x 60μm
Sub-Pixel size	20μm x 60μm
Sub-Pixel Aperture ratio	40%
Circuit size area	36μm x 20μm
Number of pixels	2.073.600

Each pixel is divided into three equal subpixels, each corresponding to a basic color red, green and blue (RGB). The three subpixels, placed one next to the other,

will produce a square pixel of 60x60μm. The aperture ratio of the OLED subpixel is the ratio of the OLED to the total area of subpixel. The maximum current that the circuit will produce is 2.5μA. The range of V_{data} voltage is 2 to 8 Volts on IGZO model simulations and 2 to 4 Volts on LTPS model. Furthermore, the V_{scan} pulse has a constant value of 12Volts.

Table 6 shows the specifications that the proposed screen will satisfy and they correspond to a 5.2-inches Full High Definition (FHD) display. The design is similar to high end mobiles display like Samsung and Huawei.

4.4 Pixel Response Time Analysis

One of the biggest challenges of the display technology is to improve the image quality emitted by the display. One solution to this challenge was to increase the scanning frequency of the image frame (Frame Rate - FR). The frame rate is the number of frames or images that are projected or displayed per second.

The increase of the frame rate has the impact on reducing the pixels' programming time and the image refresh time (frame time). However, the limited programming time, has made many of the proposed pixel's topologies, inapplicable to high performance displays. [28]

An AMOLED display is a line-at-a-time programming display. This means that all pixels of the same line are programmed simultaneously when the scan signal (V_{SCAN}) is applied to them. The available programming time of the pixels (t_{prog}) depends on the frame rate (FR) of the screen and the number of the lines of pixel's table (n_{rows}), as is shown by the following formula:

$$t_{prog} = \frac{1}{FR \cdot n_{rows}}, \tag{4.6}$$

The maximum frame rate that a screen can achieve, depends on the R-C delay of the V_{SCAN} signal diffusion lines and of the interconnections, as well as on the response time of the pixels, as shown in fig. 4.4.

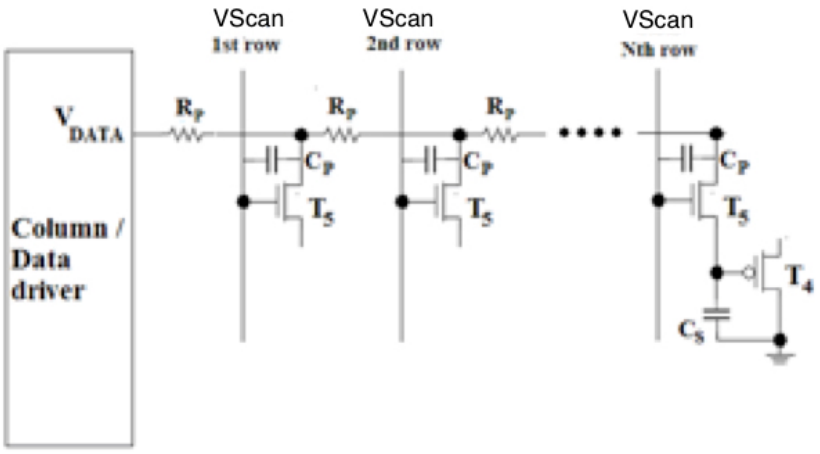


Fig. 4.4: Equivalent response time calculation of pixels circuit (settle time).

The frame rate can be calculated by the below equation:

$$FR = \frac{1}{(t_{line} + t_{settle} + t_{linedischarge}) n_{rows}} \quad (4.7)$$

In the above formula, t_{line} is the response time of the line, t_{settle}, the response time of the pixel, $t_{discharge}$, is the discharge time of lines and pixels and n_{rows} is the number of matrix rows which is equal to 1080 in the case of a FHD display format. The discharge time is the required time that is needed by the parasitic capacitances of signal transmission lines to be discharged before the new pulse of the data voltage comes from the block column drivers. The discharge time is very short compared to the line and pixels response times, so it will not be taken into account in the following calculations.

In fig. 4.4, the symbols, R_P and C_P, represent the parasitic resistances and capacitances of the transmission lines of signals respectively, as well as the connections between them. The Rp - C_P delay of signal transmission lines can be modeled by the line time, t_{line}. More specifically, the t_{line} parameter is the time the SCAN signal needed to cause the transistor switches (T1) of all pixels of the line to go to the "ON" state. The parasitic capacitance C_P created by the overlap of the SCAN signal transmission line (SCAN line) and data (Data line) and the parasitic

gate capacitance - drain of the transistor T1 each pixel. Therefore, the parasitic capacitance C_P will be given by the following formula:

$$C_p = C_{ox}\left(W_{T1}CL_{ov} + A_{l,ov}\right) \quad (4.8)$$

where the capacitance C_{ox} of the oxide of the gate of T1 per unit area, W_{T1} width of the channel of T1, L_{ov} the length of the region where the gate with the drain of T1 overlap and $A_{L,\,ov}$ is the total overlap area between the SCAN signal line and the data signal line.

The transistors are constructed with IGZO TFT technology which can produce self-aligned transistor. This means that the parasitic capacitances due to the overlapping regions of the gate and drain is too small relatively to the parasitic capacitances due to the overlap of signal transmission lines. Thus, for the signal transmission lines of 3μm thickness, with capacitance oxide (C_{OX}) that equals to 10nF/cm^2 and a channel width of T1 equal to 4um, the parasitic capacitance C_P is estimated to be equal to 0.3 pF, and the equivalent line impedance is equal to 12Ω. The time of the voltage signal to rise from 10% to 90% of its final value at any given node is considered, and as a result the line time t_{line} is 2.2 times greater than the constant of the line time. Therefore, the line time will be given by the following formula:

$$t_{line} = 2{,}2\ C_p R_p \frac{m(m+1)}{2} \quad (4.9)$$

where m, is the number of the columns in the display matrix. For a Full High Definition (FHD) display with 1920 columns, the line time is estimated to be equal to 0.2μs=200ns.

The pixel response time defined as the time that the voltage in the storage capacitor is needed to vary only 5% of the final value (5% settle time). The pixel response time is dependent on the capacity of the storage capacitor (Cs), on the ON resistance of transistor – T1 switch ($R_{ON,\,T1}$), on the parasitic gate capacitance - source of the driving transistor T2 ($C_{GS,\,T2}$) and on the parasitic capacitance C_P, as shown by the following equation:

$$t_{settle} = 3\left(C_p + C_{GS,T2} + C_S\right)\left(R_{ON,T1} + R_p\right) \quad (4.10)$$

As can be seen from the relation (4.10), the storage capacitor capacitance value plays a very important role in the pixel response time. The minimum value of the capacitor C_s is given by the equation:

$$C_S = I_{off}\frac{\text{Frame Time}}{\text{Grayscale}} \quad (4.11)$$

where I_{off} is the leakage current of the n-type TFT. Grayscale is the ratio of the data voltage swing (8V in our design topology) to 256 gray levels, which corresponds to 8-bit of the FHD-screen colors. The leakage current of the n-type transistor was measured to be equal to 10^{-13}A~0.1pA, as is shown in fig. 4.5.

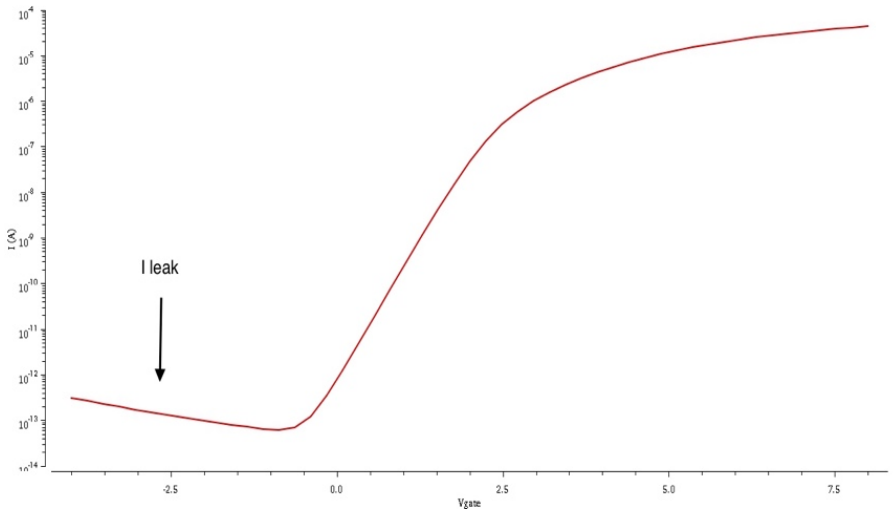


Fig 4.5: DC analysis voltage gate swing from -3Volt to 8Volts and the logI_D , to find the I_{leak}

Applying these values to equation (4.11), it is estimated that the minimum value of the storage capacitor is 80fF. In the design of the proposed pixel, the capacity of the storage capacitor was chosen to be equal to 100fF, to ensure that the data voltage stored on it will remain stable throughout the light emission phase, which lasts 6us.

Continuing the analysis, the equivalent resistance line R_P will be ignored and will not be included in the calculations. Finally, the gate– source capacity of the T2 is equal to 70fF. Applying these values in equation (4.10), it is estimated that the response time of the new pixel is 0.400μs = 400ns.

The two signals that the topology have, are the Vdata and Vscan. Vscan has a stable value equal to 12 Volts and it's very important that this value is greater than $V_{data}+V_{th}$. The Vdata signal has a range of different values because our purpose is to produce a variety of current values at the output from the driving TFT.

Moreover, it is essential that the Vdata pulse rises before the Vscan pulse. Respectively, the Vscan has to fall first and then the Vdata.

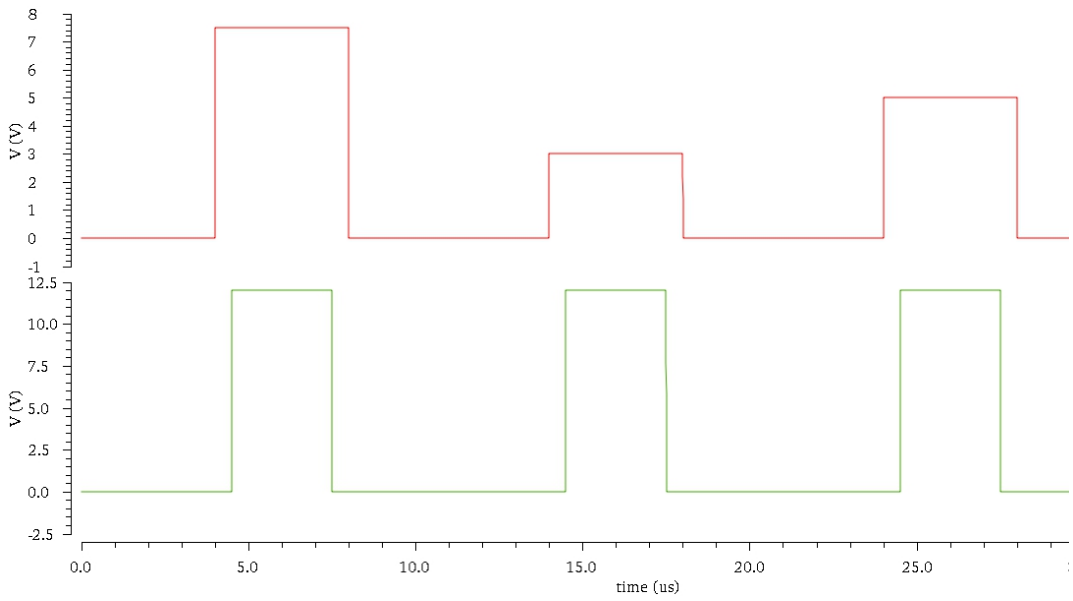


Fig 4.6: Vdata and Vscan pulses. The upper is the Vdata and the lower is the Vscan

In the upper graph (fig. 4.6), the red color shows the Vdata and every V_{data} pulse has 4μs width. The other pulse with the green color shows the Vscan pulse, which has 3μs width. The Vdata pulse preceded to Vscan by 500ns and the Vscan pulse is following. The same thing happens during the falling of the pulses. First, the

Vscan goes low and after 500ns the Vdata also falls. The rising and the falling time are set to 2ns, and in this way they are too small and negligible. For instance, the first Vdata pulse with high value 7 Volts, starts at 4^{rth}μs and goes down at 8^{th}μs. On the other hand, Vscan starts at 4.5μs and goes down at 7.5μs. The programming time is the time that BOTH these two pulses are "up", so in this case the programming time is 3μs.

In the next chapter, the simulation results from our proposed circuit with a IGZO model and a LTPS model are presented. All the simulations have been made with *virtuoso cadence*. The basic simulation has been made for Voltage-threshold, as well as, mobility field variations. Furthermore, we present the power consumption of the proposed circuit in both models and in the end the LAYOUT of the proposed pixel design.

CHAPTER FIVE

SIMULATION RESULTS

5.1 Introduction

The main disadvantage of the TFTs technology is the instability of the threshold voltage and carriers mobility. For that reason, we have chosen to run simulations for different values of threshold voltage (V_{th}) and high field mobility (MU0).

Fig. 5.1 shows the time response analysis for three different data voltage values. As we can see the response of the pixel is very quick, either if the voltage data increases or decreases. Also, the change of voltage at the capacitor can be direct, without the need to discharge it firstly. From the response analysis, it was possible to measure the settling time, the minimum value of storage capacitor and the range of Voltage data values.

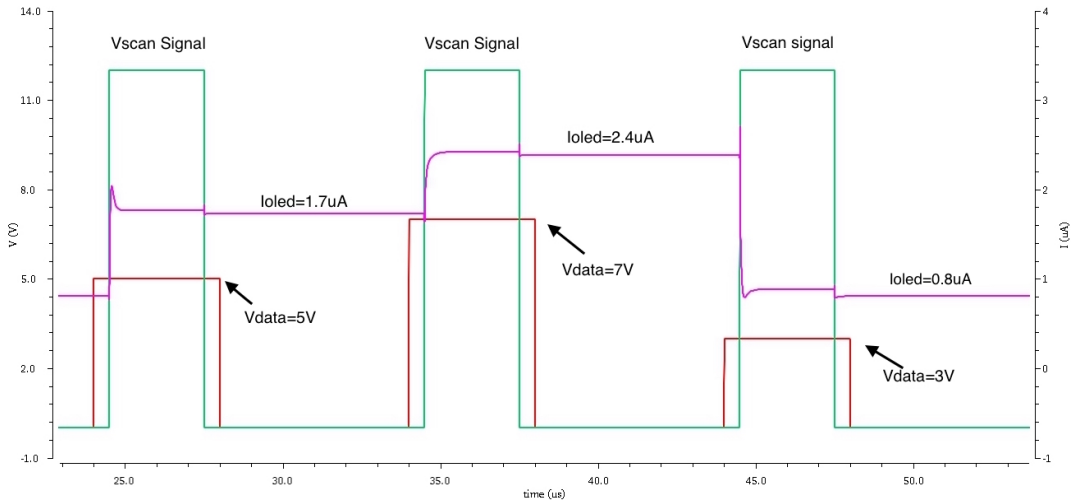


Fig. 5.1: Time response analysis for three different Data Voltage values

5.2 Indium Gallium Zinc Oxide (IGZO) model

As we have already described in chapter 1.5.3, the indium gallium zinc oxide, IGZO, is the latest technology on TFTs displays. An advantage of using this model technology is the less power consumption. In our model the threshold voltage is equal to 0.5V and the electron mobility (MU0) is equal to 11cm^2/V·s.

5.2.1 Threshold Voltage variations for IGZO model

The performance of the proposed pixel topology will be exported from the simulation results of our circuit. Fig. 5.2 shows the results of a DC simulation of pixel for V_{Data} from 1 volt to 8volts, and for other threshold voltage values. The values that the threshold voltage have, are ±30% and ±15% from the nominal threshold voltage of our model (V_T=0.5V). The above figure also presents the deviation that the current has in V_{Data} swing. As we can see, the current deviation for the OLED is only ±60nA, which means that the error is only 2.6%, compared to the nominal threshold voltage (V_{th}=0.5V) of our model.

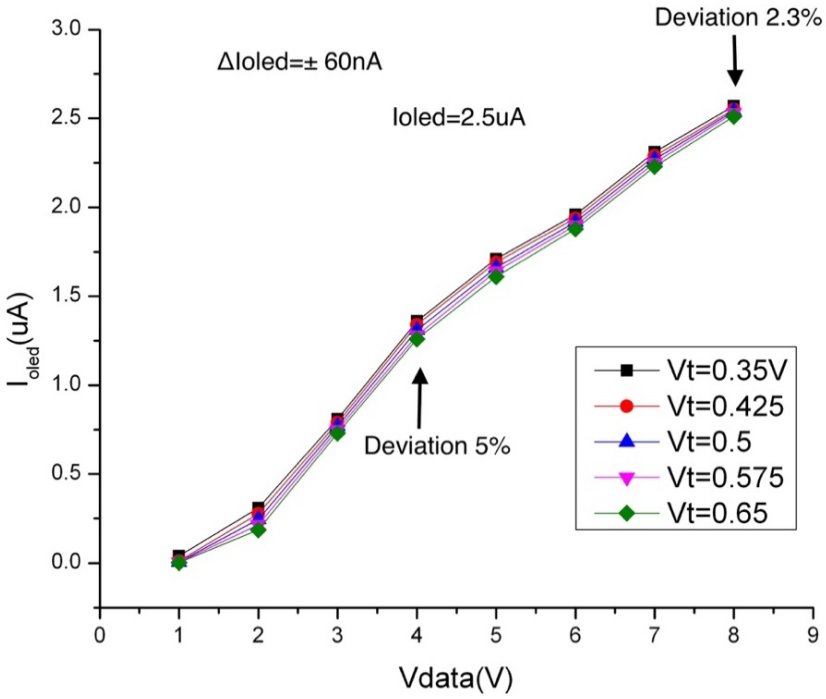


Fig 5.2: Dc analysis simulation results of the proposed pixel design for Data voltage swing from 1-8V and for threshold-voltage variation of ±75mV and ±150mV from its nominal value of 500mV

These results show that the pixel circuit works great under voltage threshold variations. Also, they show that the output current I_{OLED} is independent from the threshold voltage of the TFT.

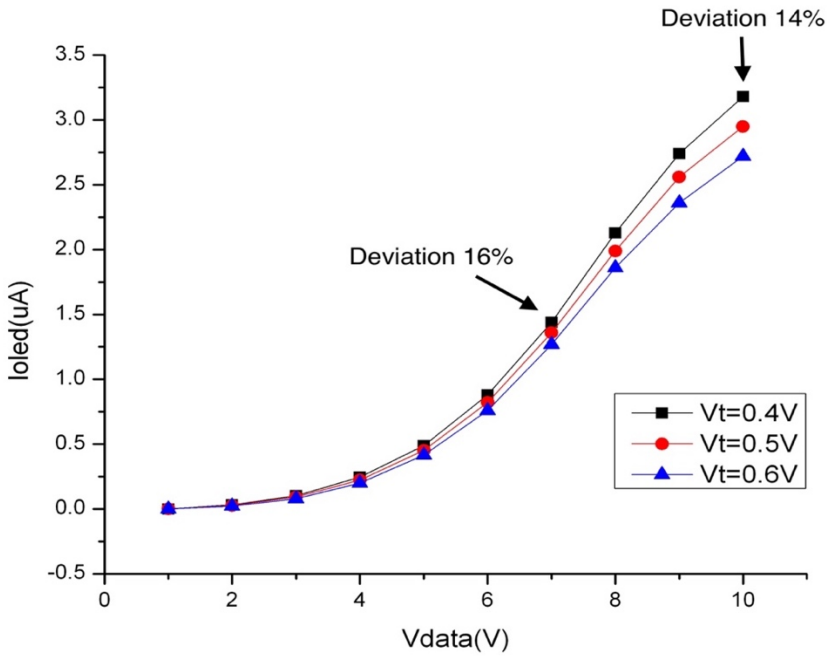


Fig 5.3: Dc analysis simulation results of the conventional pixel design 2T1C for Data voltage swing from 1-10V and for threshold-voltage variation of ±100mV from its nominal value of 500mV.

In order to confirm the improvement of the new pixel topology for threshold-voltage compensation technique, the conventional 2T1C pixel circuit has been designed using the same IGZO TFT technology and the same dimensions of TFTs.

As is shown in fig. 5.3, the conventional 2T1C pixel design has noticeable deviation through the voltage data swing from 1 Volt to 10 Volts. The deviation is always bigger than 14%, which means that the output current is not the current we planned to have. Also, the I_{oled} is depending to threshold voltage of the transistor in a significant point.

The fig. 5.4 shows the percentage output current variation comparing between the proposed pixel circuit and the conventional 2T1C pixel design. The proposed pixel exhibits an error between 2% and 8%. The 8% current error locates for very small Voltage Data values, and as the voltage data increases the current error decreases and goes to 2.3%. On the contrary, the conventional 2T1C pixel design

presents an error that starts from 60% for small OLED currents and decreases to 13% for High OLED currents.

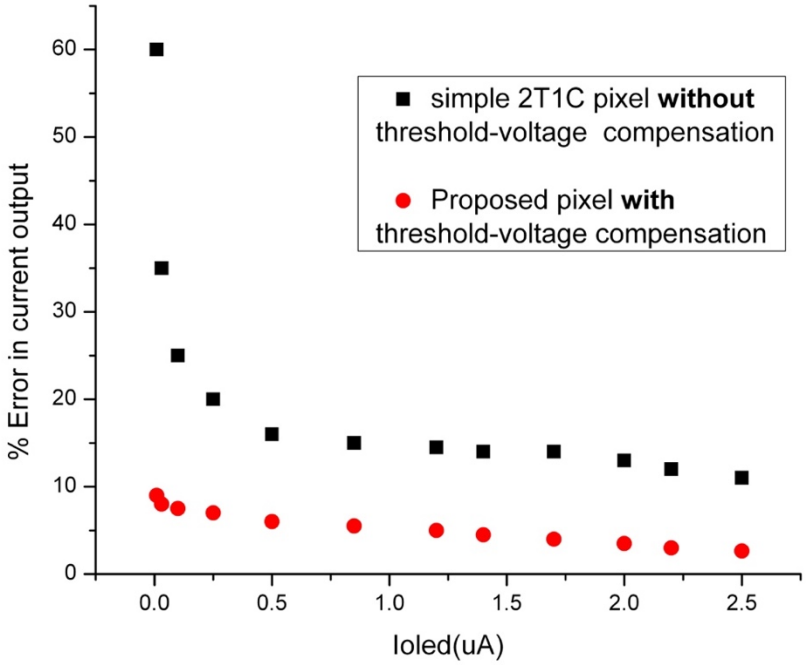


Fig. 5.4: Comparison of the OLED current error due to the threshold voltage variation between the proposed pixel design and the conventional 2T1C pixel design

The comparison of the two pixels' design reflects that we achieved to design the conventional 2T1C pixel, using the new threshold-voltage compensation technique. As we can see, the output current error is more stable. It is under 10%, while in the maximum value of the current (2.5uA), it is 2.3% respectively. On the other hand, in the conventional pixel design the output current error has a much bigger deviation.

5.2.2 Carriers mobility variations for IGZO model

The IGZO model is 20 to 50 times faster than a-Si in electron mobility. The electron *mobility* is the ability of an electron to move through semiconductor, in the presence of applied electric field. The standard unit for mobility is $cm^2/V{\cdot}s$. A

typical value for mobility in LTPS model is 90-100 $cm^2/V \cdot s$ and for IGZO model is 10-20 $cm^2/V \cdot s$

$$V_d = \mu \cdot E \quad \Rightarrow \quad \mu = \frac{E}{V_d} \tag{5.1}$$

where, E is the magnitude of the electric field applied to a material, V_d is the magnitude of the electron drift velocity (in other words, the electron drift speed) caused by the electric field, and μ is the electron mobility. [29]

Fig 5.5 presents the results of a DC simulation of pixel for V_{Data} from 1 Volt to 9 Volts and for three high electrons mobility values. The graph reveals the nominate model value MU0= $11cm^2/V \cdot s$ as well as two other values at ±20%, which means for mobility ± $2cm^2/V \cdot s$ approximately. The deviation of the current output is ± 150nA and it is equal to 8% error. Also the error at the output has a small variation from 14% for small currents and finally goes to 8% for 2.5uA.

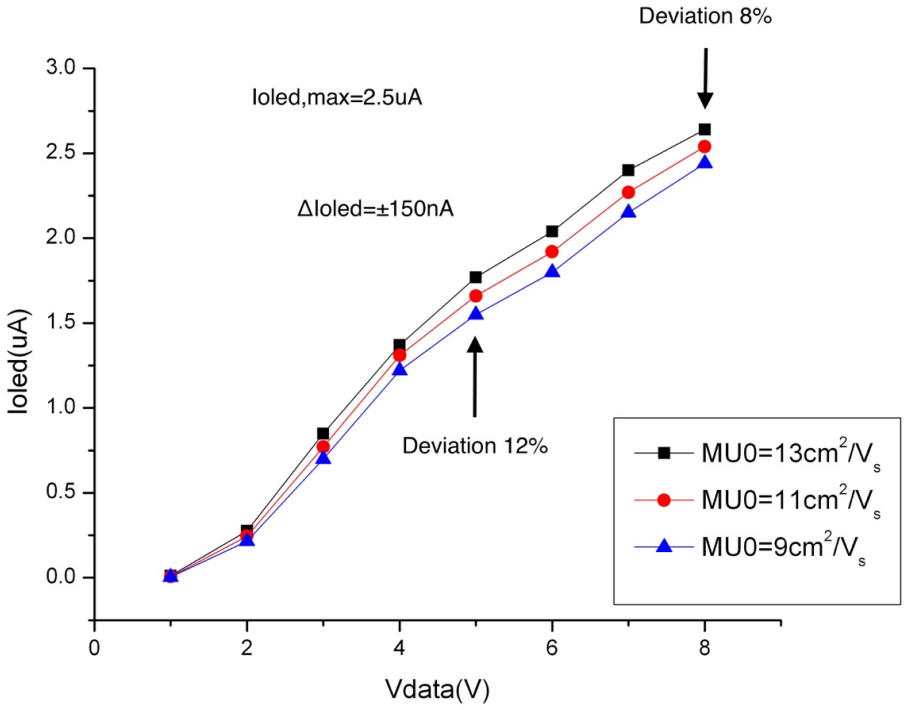


Fig 5.5: Dc analysis simulation results of the proposed pixel design for Data voltage swing from 1V to 8V and high mobility variation of ±2 cm^2/Vs from its nominal value of 11cm^2/Vs

In order to establish the feasibility of the new threshold-voltage compensation technique, the conventional 2T1C was designed using the same IGZO TFT technology. The dimensions of the TFTs were exactly the same in both two measurements. Fig 5.6 shows the error current comparison between the proposed pixel design and the conventional 2T1C.

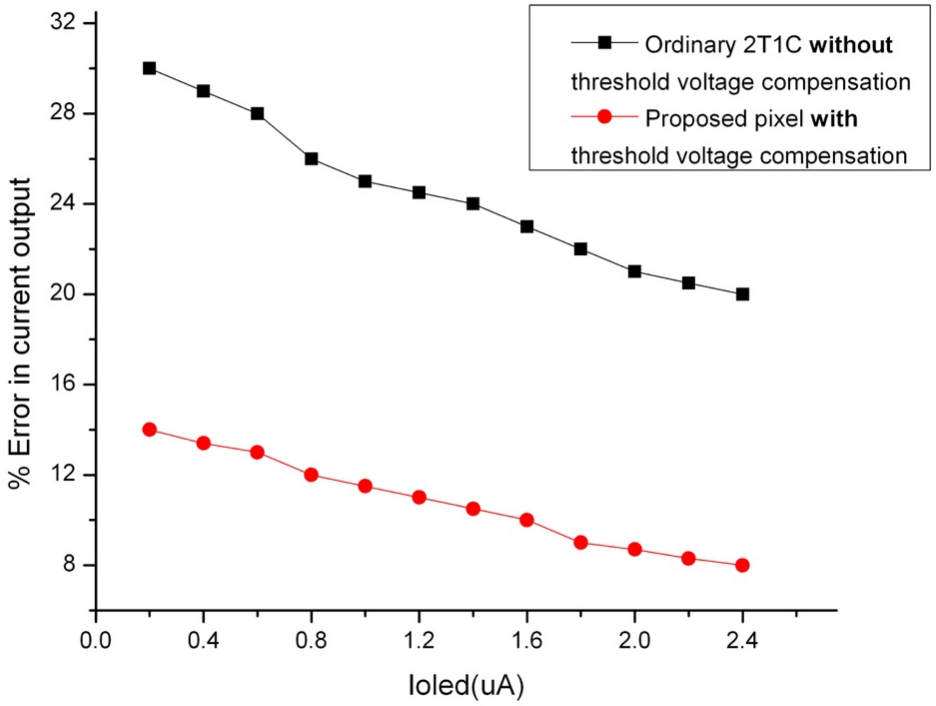


Fig 5.6. Comparison of the OLED current error due to the high mobility variation (MU0) between the proposed pixel design and the conventional 2T1C pixel design in the IGZO model

The graph in fig. 5.6 shows the current error in output of the Driving TFT I_{oled}. As we can see the variation of the proposed pixel is approximately 14% for small currents and decreases steadily to the maximum current which is 2.4uA and reaches the minimum variation which is 8%. On the other hand, the conventional 2T1C pixel design has a much bigger variation through the current swing from 0.2uA to 2.4uA.

For small currents the error at the output of the driving TFT is approximately 30%, and the final variation value reaches to 20% at 2.4uA.

So, in that way, we checked the deviation between the proposed pixel design and the conventional pixel design for three high electron mobility values.

Table 7. Table of LTPS parameters for n-type TFT

	Symbol	Parameter description	Unit	Value
1	ASAT	Proportionality constant of Vsat		0.9
2	AT	DIBL parameter 1	m/V	1.3e-8
3	BLK	Leakage barrier lowering constant	-	0.001
4	BT	DIBL parameter 2	m/V	1.9e-6
5	CGDO	Gate-drain overlap capacitance per meter channel width	F/m	0
6	CDSO	Gate-source overlap capacitance per meter channel width	F/m	0
7	DASAT	Temperature coefficient of ASAT	1/°C	0
8	DD	Vds field constant	M	2.0e-7
9	DELTA	Transition width parameter	-	4
10	DG	Vgs field constant	M	1.3e-7
11	DMU1	Temperature coefficient of MU1	cm^2/Vs°C	0
12	DVT	The difference between VON and the threshold voltage	V	0
13	DVTO	Temperature coefficient of VTO	V/°C	0
14	EB	Barrier height of diode	eV	0.68
15	ETA	Sub-threshold ideal factor	-	6.6
16	ETAC0	Capacitance sub-threshold ideality factor at zero drain bias	-	ETA
17	ETAC00	Capacitance sub-threshold ideality factor of drain bias	1/V	0
18	I0	Leakage scaling constant	A/m	6
19	I00	Reverse diode saturation current	A/m	150
20	LASAT	Coefficient for length dependence of ASAT	M	0
21	LKINK	Kink effect constant	M	1.5e-5
22	MC	Capacitance knee shape parameter	-	3
23	MK	Kink effect exponent	-	1.1
24	MMU	Low field mobility exponent	-	3
25	MU0	High field mobility	cm^2 / Vs	90
26	MU1	Low field mobility parameter	cm^2 / Vs	1.7e-3
27	MUS	Subthreshold mobility	cm^2 / Vs	0.55
28	RD	Drain resistance	Ω	500
29	RDX	Resistance at series with Cgd	Ω	0
30	RS	Source resistance	Ω	500
31	RSX	Resistance at series with Cgs	Ω	0
32	TNOM	Parameter measurement temperature	°C	25
33	TOX	Thin-oxide thickness	m	1.2e-7
34	VFB	Flat-band voltage	V	-0.1
35	VKINK	Kink effect voltage	V	6.6
36	VON	On-Voltage	V	0
37	VTO	Zero-bias Threshold voltage	V	1.3

5.3 Low-Temperature Polycrystalline Silicon –LTPS – model

The Low-Temperature Polycrystalline Silicon (LTPS) model has much bigger threshold voltage compared to the IGZO model. The threshold voltage in the LTPS model is 1.3V while in the IGZO model is 0.5V, as shown in table 7. Furthermore, the high field mobility is also much bigger in the LTPS model (MU0=90cm^2/Vs) compared to the IGZO which is only 11cm^2/V·s. In the LTPS model we performed the exact same specifications as in the IGZO model which we have described in the previous paragraphs [30].

In LTPS model the V_{data} signal has a much smaller voltage swing, from 2V to 4V. So, in this way, there is less power consumption for the circuit but it is more difficult to achieve the exact amount of current at the output.

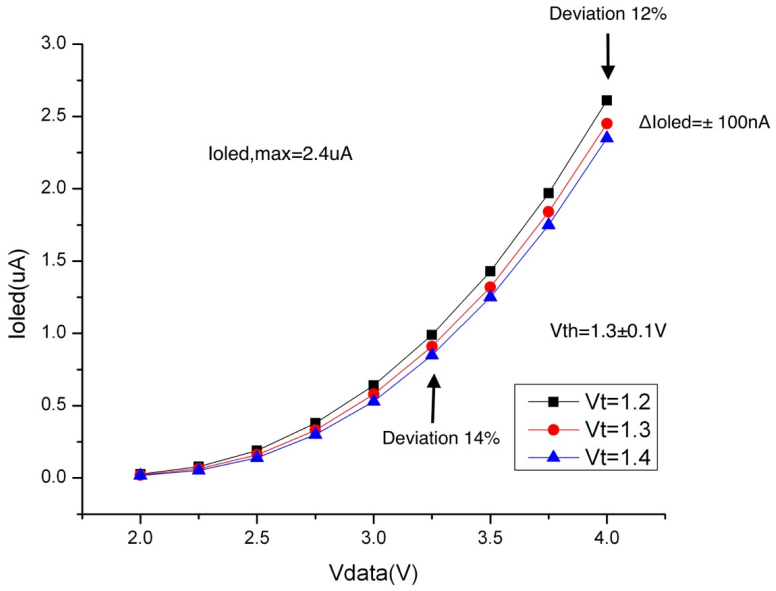


Fig. 5.7 DC response of the proposed pixel design for a data voltage swing from 2V up to 4V and for threshold-voltage variations of ±100mV. For this threshold-voltage the deviation of the OLED current is equal to 2.4uA indicating an error of 12%

5.3.1 Threshold Voltage variations for LTPS model

For this simulation, the threshold voltage range was ±15% from the nominal threshold voltage value of our model (V_{th} = 1.3V). The following figure presents the deviation of the current in V_{data} swing from 2V to 4V. The graph shows that the current deviation for the OLED is only ±100nA, which means that the error is 12%, compared to the nominal threshold voltage value of our model.

In order to better check the results, the conventional 2T1C was designed using the same LTPS TFT technology. The dimensions of the TFTs were exactly the same in both two measurements. Fig. 5.8 shows the error current comparison between the proposed pixel design and the conventional 2T1C. The proposed pixel gradually declines from 20% error in small currents and finally goes to 12% at 2.5uA which is the maximum data Voltage. On the other hand, the conventional 2T1C pixel design has significantly larger variation at the output current. It starts from 50% for small currents and in the end goes to 20% error in the output.

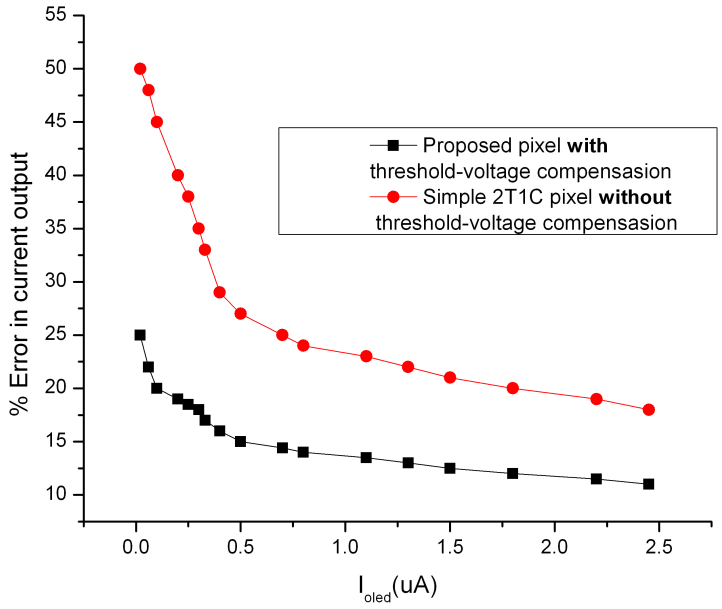


Fig 5.8. Comparison of the OLED current error due to the threshold voltage variation between the proposed pixel design and the conventional 2T1C pixel design

5.3.2 Carriers mobility variations for LTPS model

As we have already mentioned in 4.5.1b paragraph, the electron mobility is the ability of an electron to move through semiconductor, in the presence of applied electric field. A typical value for mobility in LTPS model is 90 to100 $cm^2/V{\cdot}s$. As we can see, Fig 5.9 presents the results of a DC simulation of the pixel for V_{data} from 2V to 4V and for five high electrons mobility values. The graph presents the nominate model value MU0= 90 $cm^2/V{\cdot}s$, as well as, four other values at ±10% and ±20% respectively, which means mobility values of ±10$cm^2/V{\cdot}s$ and ± 20$cm^2/V{\cdot}s$ approximately. The deviation of the current output is ± 150nA and it is equal to 10% error. Also, the error at the output has a small variation from 18% for small currents.

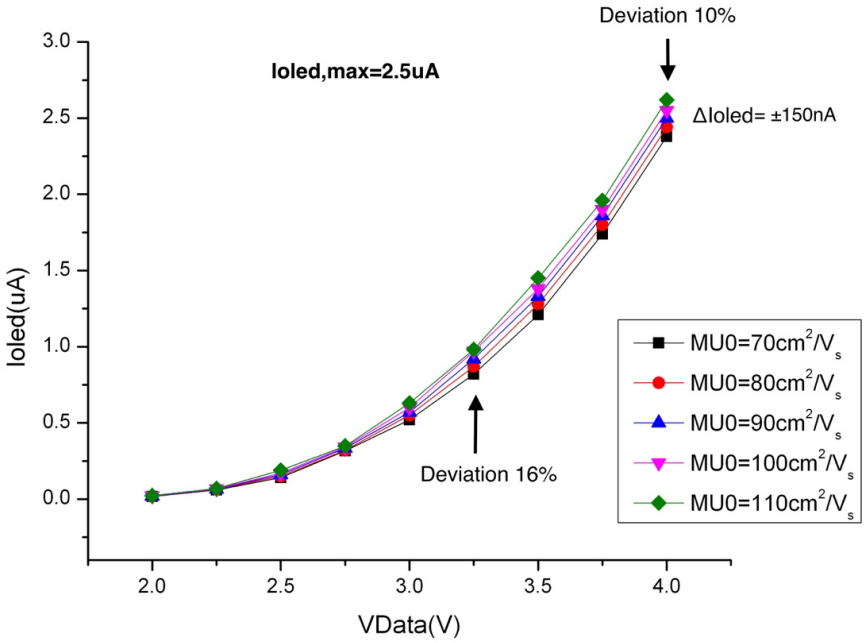


Fig. 5.9. DC response of the proposed pixel design for a data voltage swing from 2V up to 4V and high mobility variation of ±10 cm^2/Vs and ±20 cm^2/Vs from its nominal value of 90cm^2/Vs. For this high mobility variation, the deviation of the OLED current is equal to 2.4uA indicating an error of 10%.

In order to establish the feasibility of the new threshold-voltage compensation technique, the conventional 2T1C was designed using the same LTPS TFT

technology. The dimensions of the TFTs were exactly the same in both two measurements. Fig. 5.10 shows the error current comparison between the proposed pixel design and the conventional 2T1C. The proposed pixel declines from 20% error in small currents and finally goes to 10% at 2.5uA, which is the maximum Voltage data. On the contrary, the conventional 2T1C pixel design has an error at the output over 25% in all V_{data} swing.

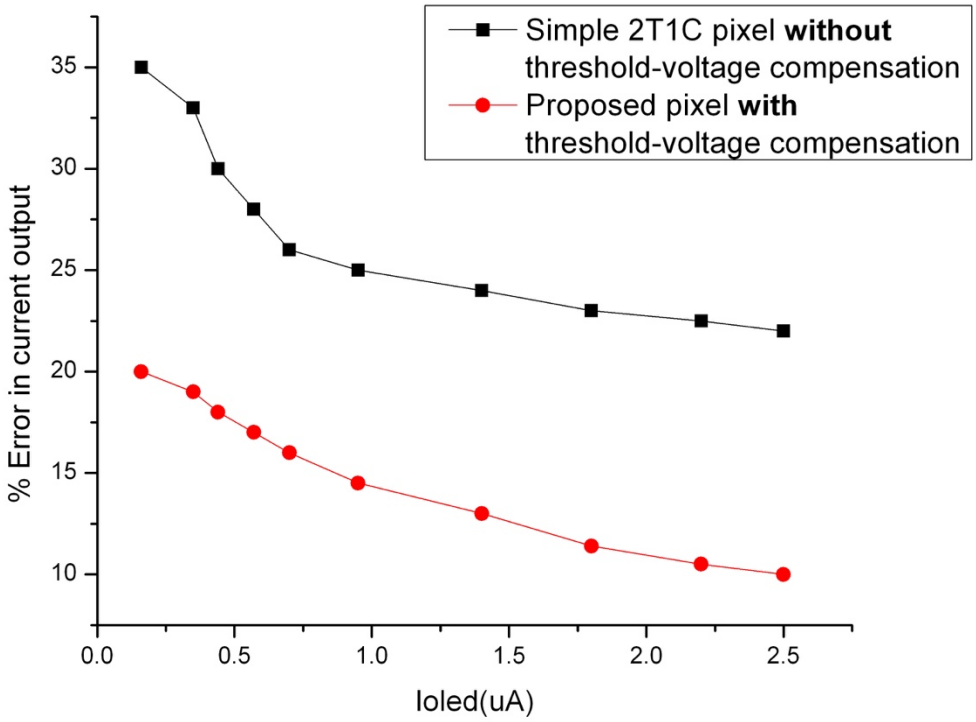


Fig 5.10. Comparison of the OLED current error due to the high mobility variation (MU0) between the proposed pixel design and the conventional 2T1C pixel design in the LTPS model

5.4 LAYOUT

For the layout we used the layout XL environment from the virtuoso cadence suite. The difficult part of the design was the extremely small area of the pixel, due to the specification of the display, as seen in Table 6 (see §4.2). Specifically, as the area of the pixel had to be 60x20 um^2 and the aperture ratio is 40%, the available area for the circuit was only 36x20um^2.

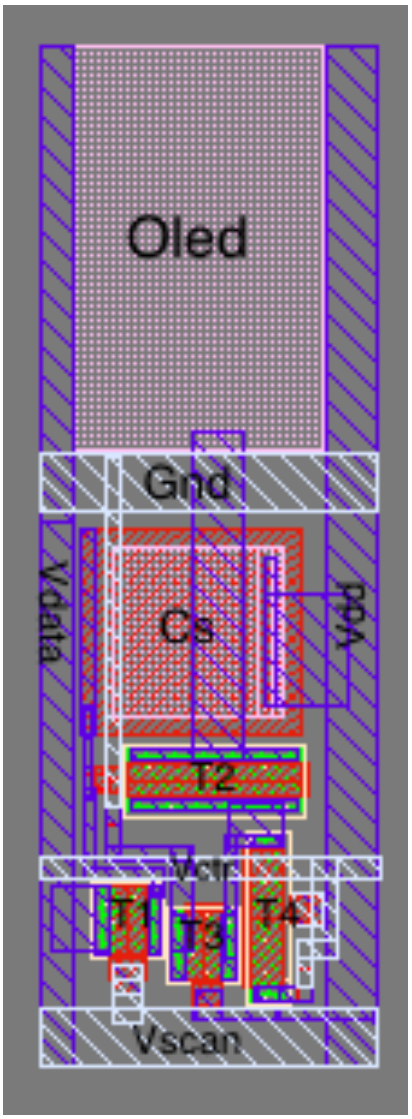


Fig. 5.11. LAYOUT presentation of the proposed sub-pixel design

The materials used for the pixel layout were two kinds of metal (MET1 & MET2) and a Poly-Silicon (POLY1).

The V_{data} signal is located on the left side of the pixe is on MET1. This metal is 60um wide and 2.5um long. The supply Voltage of the circuit (Vdd) is located on the right side of the design and has the same dimensions, except for the length of the Vdd, which is 3.2um.

The Vscan signal is located on the bottom side and it is on MET2. This is because the two lines have to be drawn by different material, and in this case the one is overlapping the other. The Vscan is 20um long and 3um wide. The Vctr is a constant power supply (Vctr=3V) and give power to the diode connected TFT (T4). This is what we really want, in order to have at the output Vs=Vctr-Vt.

Transistor T2 and T4 have to be placed closely in the pixel design so that the assumption for these two transistors to share the same threshold voltage to be valid.

Finally, at the top of the circuit design is the Ground (Gnd), which is also on MET2, that is 3.5um wide.

The Fig 5.11 shows the Layout presentation of a sub-pixel. This subpixel is 60um wide and 20um long. Every sub-pixel is 8-bit gray-scale, so it can produce 2^8=256 colors. That is only for one sub-pixel.

In Fig 5.12 is shown the Layout presentation of a pixel. The dimensions of one pixel unit is 60x60 um. As one pixel is the combination of three sub-pixels and each of them has gray-scale 8-bits, so 2^8=256 different colors for every sub-pixel. Using eight bits for each RGB color, we can generate roughly 256^3=16.77 million colors that the pixel can produce (256 for Red, 256 for Blue and 256 for Green).

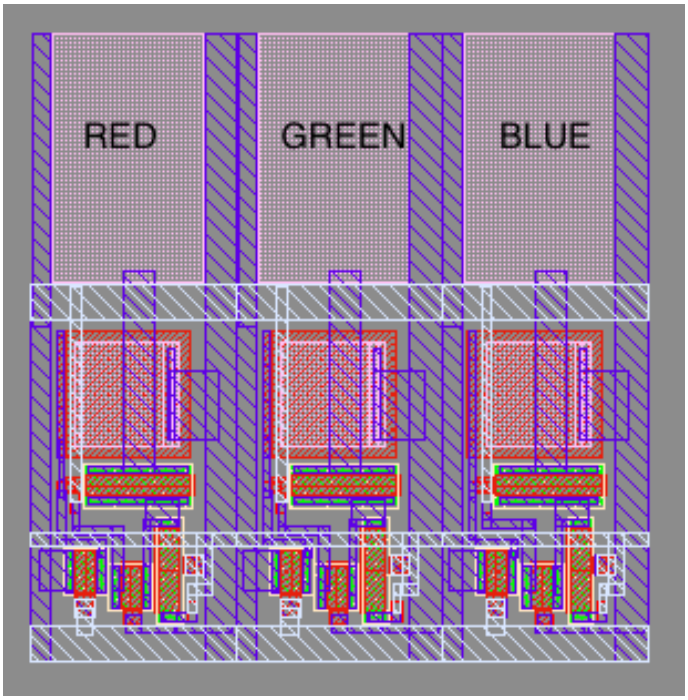


Fig. 5.12 LAYOUT presentation of the proposed pixel design

5.5 Power Consumption

The total power consumption of a digital system consists of a dynamic and a static component:

$$P_{tot}=P_{stat}+P_{dyn} \quad (5.2)$$

In order to explore the power consumption of the proposed pixel circuit we had to examine two cases. The first case is when the display is at a 100% brightness, which is the worst case for static power consumption. This means, that all pixels of the display are permanently "ON" and it also means that there will only be static power consumption.

The second case we have to examine is the 50% brightness of the display, which is the worst case for dynamic power consumption. This is due to the fact that half of the display's pixels will be "ON" and the other half will be "OFF".

5.5.1 Full brightness

In order to calculate the power consumption in the first case (100% brightness), where all the pixels of the display are "ON", only the static power exists, as there is no variation in the pixel's mode.

The static power of the sub-pixel, is given by,

$$Pstat_{,sub\text{-}pixel}=V_{dd}*I_{oled}, \quad (5.3)$$

where V_{dd} is the power supply of the circuit and I_{oled} is the current of the pixel.

The power supply (Vdd) for the IGZO model simulation is 10Volts and for the LTPS model simulation is 6 Volts. In both models the maximum Ioled is 2.4uA.

In order to find the total power consumption of the pixel we have to multiply the static power of the sub-pixel three times. This is due to the fact that the pixel consists by three sub-pixels.

$$Pstat_{,pixel}= 3* Pstat_{,sub\text{-}pixel} \quad (5.4)$$

Finally, the power consumption for the static mode (100% brightness) for the IGZO model is 72uW and for the LTPS model it is 43.2uW. This value difference is due to the fact that the LTPS model needs a much lower power supply. The power consumption at LTPS model saves 66.7% more than the IGZO model.

5.5.2 Half brightness

This is the worst possible case for the dynamic power consumption. It is the 50% brightness case, also known as "Checkboard", because one pixel is "ON" and the neighboring pixel is "OFF".

The 50% brightness rate of the display is given by,

$$Ptot =100\%Pdyn+50\%Pstat, \quad (5.5)$$

where the Pstat, is the static power consumption that had been analyzed earlier and the Pdyn is the dynamic power consumption. The Pdyn of the sub-pixel is given by:

$$Pdyn_{,sub\text{-}pixel}=C_{tot}*V^2*f*Nrow, \quad (5.6)$$

where V, is the value of voltage to charge the capacitor (approximately is the Vdata value), f is the frequency of the circuit (in our case is the frame rate) and finally,

Ctot is the sum of storage capacitor Cst and the gate-source capacitor of the driving TFT (T2).

$$Ctot=Cst+Cgs_{,T2} \tag{5.7}$$

$$Cgs_{,T2}=\frac{3}{2} * W * L * Cox \tag{5.8}$$

To calculate the gate-source capacity of the driving TFT we multiple the width and the length of the transistor and also the Cox of the model. The width is 10um and the length is 2um.

The Cox in the IGZO model is $2.2*10^{-7}$ F/um^2 and in the LTPS model is respectively $1.2*10^{-8}$ F/um^2.

$$Ptot_{,pixel}=3*Ptot_{,sub\text{-}pixel} \tag{5.9}$$

In order to find the total power consumption of the pixel we have to multiply the total power consumption of the sub-pixel three times. This is due to the fact that the pixel consists by three sub-pixels.

By calculating the total power for the IGZO model is 38.4uW and for the LTPS model is 22uW.

5.5.3 Conclusions

Summarizing, as we can see, with the LTPS model there is remarkably lower power consumption. And more analytically in the first case of full brightness it is 66.7% lower than the IGZO model. In the second case of 50% brightness the power saving is higher than the first case and reaches almost 75% power saving. All these results are presented in the table below.

Table 8. Power consumption in the case of full and half brightness

	100% brightness	50% brightness
IGZO	72uW	38.4uW
LTPS	43.2uW	22uW
Power saving	66.7%	74.5%

CHAPTER SIX
CONCLUSIONS AND DISCUSSION

6.1 Comparison with other circuits

In this paragraph we present four different designed circuits which have been previously presented by researchers in the area of active matrix organic light emitting diode display pixel. Subsequently, we analyze the basic features of these four circuits, their operation design and we notice differences between them and our circuit.

6.1.1 First circuit

The first circuit that that is presented and compared to our circuit, is one proposed by Lin et al. (2014). It is a simple pixel structure (see fig. 6.1a), that uses the voltage-programmed method to compensate for the electrical characteristic variations in low-temperature polycrystalline-silicon thin-film transistors and the current– resistance (I – R) voltage drop in the power line for active-matrix organic light-emitting diode displays. Based on the experimental results, the functionality of the pixel circuit can be operated correctly during each operation phase. Moreover, the pixel current exhibits high uniformity against the threshold voltage and mobility variations in the driving TFT. [31]

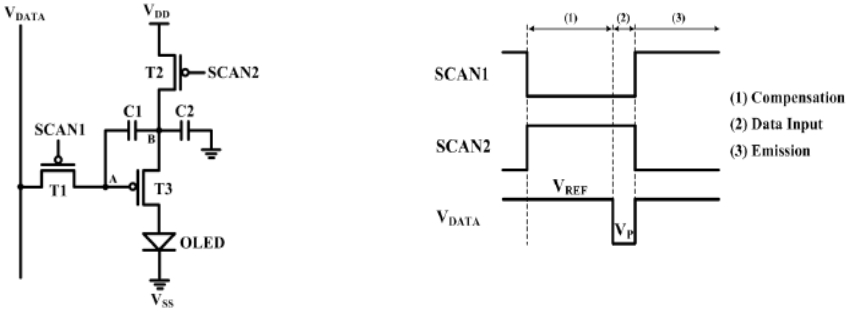


Fig. 6.1. (a) Pixel structure and its (b) timing diagram

Fig. 6.1(b) schematically shows the timing diagram of pixel circuit control signals. The proposed pixel utilizes all p-type LTPS TFTs, including one driving TFT (T3), two switching TFTs (T1 and T2), and two storage capacitors (C1 and C2). The operation of the proposed circuit is divided into the compensation stage, data input stage, and emission period. In the compensation stage, SCAN1 is low to

turn ON T1, and a reference voltage (V_{REF}) is applied to node A. Meanwhile, SCAN2 is high to turn OFF T2. The voltage of node B (VB) was VDD in the previous emission period, VB is discharged to $V_{REF} + |V_{TH\_T3}|$ until T3 is turned OFF, where V_{TH_T3} is the threshold voltage of T3.

Subsequently, in the data input stage, SCAN1 remains low to turn "ON" T1 and SCAN2 remains high to turn "OFF" T2. Thus, a programming voltage (VP) is applied to node A, and by the coupling effect of C1 and C2, VB becomes

$$V_B = V_{REF} + \left|V_{TH\_T3}\right| + \frac{C_1}{C_1+C_2} * \left(V_p - V_{REF}\right) \tag{6.1}$$

At this time, T3 is turned "ON" again, and thus VB decreases by $\Delta VB(\mu T3)$, which is mainly related to the mobility of T3 because V_{TH_T3} has already been compensated in the compensation stage. Therefore, the stored voltage of C1 between VB and VA is given by

$$V_{SG\_T3} = \frac{C_1}{C_1+C_2} * \left(V_{REF} - V_p\right) + \left|V_{TH_{T3}}\right| - \Delta V_B(\mu_{T3}) \tag{6.2}$$

During the emission period, SCAN1 goes high to turn "OFF" T1 and SCAN2 goes low to turn ON T2. Thus, VB becomes VDD and VA is floated. Since C1 sustains the same stored voltage as (6.2), the drain current of T3 flows through the OLED, which can be expressed as

$$I_{oled} = \frac{1}{2}k\left(V_{SG_{T3}} - \left|V_{TH_{T3}}\right|\right)^2 =$$

$$I_{oled} = \frac{1}{2}k\left[\frac{C_1}{C_1+C_2}\left(V_{REF} - V_p\right) - \Delta V_B(\mu_{T3})\right]^2 \tag{6.3}$$

where $k = \mu_{T3} * C_{ox} * \frac{W}{L}$

Based on (6.3), the OLED current is independent of the threshold voltage of T3 and the IR voltage drop in the power line. Moreover, a pixel with higher mobility generates a larger $\Delta VB(\mu T3)$. As a result, the effect of the mobility variation of TFT can also be ameliorated using the proposed circuit. The subthreshold slope, mobility, and threshold voltage of T3 are 0.51 V/decade, 65 $cm^2/V \cdot s$, and −2.4 V.

One advantage of this design is the narrow Voltage swing in the data Voltage. It needs 2.2 to 3 Volts to achieve the maximum Ioled.

The OLED variation for ΔVt ±0.5V for the maximum Ioled is 10% and the average variation is 15%. These values are much bigger compared to our proposed pixel design.

Summarizing, the above described circuit has a lot of things similar to our proposed circuit. It has approximately the same number of TFTs, while it has one more capacitor than ours. Furthermore, this circuit presents a better stability in the electrical characteristics variation than our proposed circuit.

6.1.2 Second Circuit

The second circuit that is presented and compared to our circuit, concerns a new pixel circuit, presented by Lin, C-L. et al. (2013). This circuit uses a-IGZO TFTs for three-dimensional (3D) active-matrix organic light-emitting diode (AMOLED) displays. Consequently, the frame rate when 3D mode is adopted should be increased to 240 Hz or more. [32]

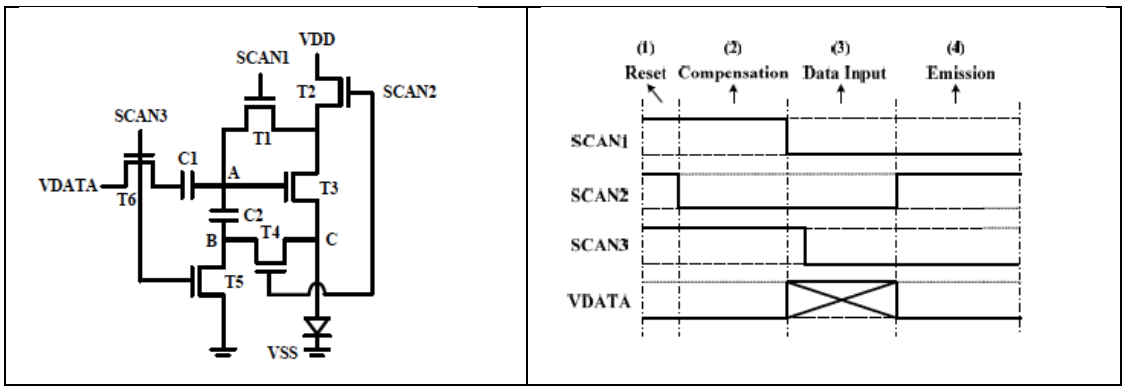


Fig. 6.2. Pixel schematic diagram and timing diagram

As the diagram in fig. 6.2 shows, six TFTs and two capacitors are adopted, including one driving TFT (T3) which determines the OLED output current and five switching TFTs which are used as a switch function.

The operating stages and compensation scheme are described in fig. 6.2. First, *reset stage,* where, all the SCANs are at a high voltage so that all the switching TFTs are in the on state which can reset the voltage of node A (VA) to VDD and

reset the voltages of nodes B and C (VB and VC) to a ground voltage (VSS). The voltage of data line is set to a reference voltage (Vref). Second, in *compensation stage*, the SCAN1 and SCAN3 maintain high voltage therefore the VB remains to VSS and the voltage of data line remains Vref. The SCAN2 goes to a low voltage to turn off T2 and T4. Since the T3 is in the diode connection structure, VA starts discharging until the driving TFT (T3) and the OLED are turned off, which is set to VTH_OLED+VTH_T3, where VTH_T3 and VTH_OLED are the threshold voltage of T3 and the OLED, respectively. By this way, the VTH_OLED and the VTH_T3 are detected and stored in the gate node of T3 in order to compensate for the decay of OLED luminance. Thirdly, during *data input stage*, the SCAN1 goes low to turn off T1 and the SCAN3 remains high to turn on T5 and T6, thus, the VB remains VSS. Simultaneously, the voltage of data line changes from Vref to a data voltage (VDATA). Due to the charge conservation, the gate voltage of driving TFT_{VG_T3} would be boosted to

$$V_{G\_T3} = V_{TH\_OLED} + V_{TH\_T3} + \left(V_{DATA} - V_{ref}\right) x \frac{C1}{C1+C2} \tag{6.4}$$

Thus, the voltage across C2 (VC2) is:

$$V_{C2} = V_{TH\_OLED} + V_{TH\_T3} + \left(V_{DATA} - V_{ref}\right) x \frac{C1}{C1+C2} - V_{ss} \tag{6.5}$$

After the data input, SCAN3 goes low to enter a holding period for other pixel rows to input their data.

Finally, in the *emission stage*, SCAN3 goes high to turn on T2 and T4 so that the driving currents (I_{OLED}) of all pixels start flowing through the OLEDs. The calculation of I_{OLED} is given by:

$$\begin{aligned} I_{OLED} &= \frac{1}{2} k \left(V_{G\_T3} - V_{TH\_T3}\right)^2 = \\ &= \frac{1}{2} k \left[V_{TH_{OLED}} + V_{TH_{T3}} + \left(V_{DATA} - V_{ref}\right) x \frac{C1}{C1+C2} - V_{ss} - V_{TH_{T3}}\right]^2 \\ &= \frac{1}{2} \mathrm{k} \left[V_{TH\_OLED} + \left(V_{DATA} - V_{ref}\right) x \frac{C1}{C1+C2} - V_{ss}\right]^2 \end{aligned} \tag{6.6}$$

where k is $\mu \cdot C_{OX} \cdot W_{T3/LT3}$. It is obvious that the item V_{TH_T3} is removed and there is an additional item V_{TH_OLED}, which is the threshold voltage of OLED to detect the

degradation of OLED. Consequently, the decay of OLED luminance is compensated which has high immunity to V_{TH} variation of driving TFT and OLED material ageing.

Compared to our pixel design, this design is more complex than ours, with more TFTs (six than four TFTs) and two capacitors than one, respectively. A serious disadvantage of the above described pixel is that it needs many signals in order to operate. On the contrary its main advantage is its high Frame rate. Its frame rate is significant approximately 240Hz (bigger than in our design which is 90Hz) and due to this, the circuit can be used in 3-D displays.

6.1.3 Third pixel

The third pixel circuit that is presented and compared to our circuit, is presented by Kim et al. (2014), and it is a novel voltage-programmed pixel circuit based on a-InGaZnO TFTs for AMOLED displays with the enhanced aperture ratio is proposed. The proposed circuit consists of 5 TFTs and one capacitor. The pixel composed of one power line (V_{DD}) and ground line (V_{SS}), two control lines (Gate1, Gate2), a capacitor C_1) and five TFTs; one pre-charge TFT (PC), two switch TFTs (SW1, SW2), a mirror TFT (MR), and a driving TFT (DR) as is shown in fig. 6.3. Moreover, fig. 6.3 shows the operational waveforms of the proposed circuit. [33]

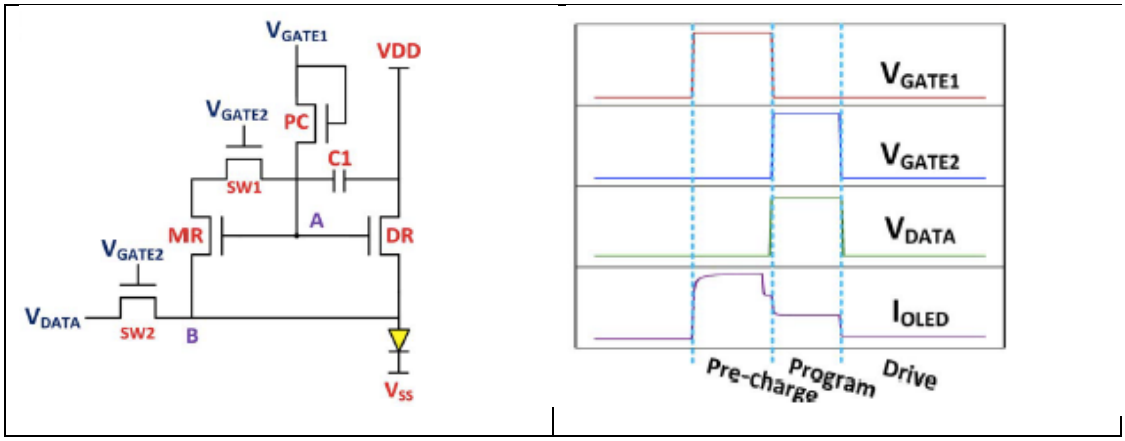


Fig. 6.3. Schematic circuit diagram and operational waveforms of the proposed pixel circuit.

The operation detail of this circuit is as following: First, during the pre-charge (PC) stage, as V_{GATE1} turns on the pre-charge TFT (PC TFT), the pre-charge TFT operates as diode because its drain and gate nodes are connected together. There- fore, the voltage at node A is determined as the high voltage level of V_{GATE1} minus the threshold voltage of PC TFT: $V_A=V_{GATE1}-V_{TH\_PC}$, which is relatively high than data high voltage, and is charged in C1.

Secondly, during the program stage, PC TFT is turned off and both the SW1 and SW2 TFT are turned on to make the diode connection for MR TFT by connecting the gate and drain of MR TFT. In this state, data voltage is applied to the node B through 2 TFT $V_B=V_{DATA}$). At the same time, C1 starts to dis- charge until the value of the gate voltage of MR and DR TFT charged in the previous stage is equal to the data voltage plus the threshold of MR TFT($V_A=V_{DATA}+V_{TH\_MR}$). Consequently, the threshold voltage of the MR TFT is programmed and stored in the storage capacitor as in (6.1).

$$V_A=V_{DATA}+V_{TH\_MR} \quad \text{and} \quad V_B=V_{DATA} \tag{6.7}$$

At last, during the drive stage, as SW1 and SW2 TFT are all turned off, and the drive TFT makes the programmed OLED current flow. In this stage, the voltage at node B is re-scaled by the voltage division between R_{ON} of DR TFT and resistance of OLED as SW2 TFT is turned off

$$V_B = \left(\frac{R_{diode}}{R_{on_{DR}}+R_{diode}}\right) * (V_{DD} - V_{SS})) + V_{SS} \tag{6.8}$$

Since is assumed that the threshold voltages of MR and DR TFT are identical, the stored voltage $V_A=V_{DATA}+V_{TH\_MR}$ in C1 to keep DR TFT turned on to make OLED current flowing independent from of DR TFT as following,

$$V_A=V_{DATA}+V_{TH\_MR} \tag{6.9}$$

$$V_B = \left(\frac{R_{diode}}{R_{on_{DR}} + R_{diode}}\right) * (V_{DD} - V_{SS})) + V_{SS}$$

$$V_{Gs} = V_G - V_S = V_A - V_B$$

$$I_{oled} = \frac{1}{2}k(V_{GS} - V_{TH})^2$$

$$= \frac{1}{2}k\left(V_{DATA} + V_{TH_{MR}} - V_B - V_{TH_{DR}}\right)^2 = \frac{1}{2}k(V_{DATA} - V_B)^2 \qquad (6.10)$$

Summarizing, the above described circuit has many things in common with our proposed circuit. It contains approximately similar number of TFTs and capacitors and it has a similar way of operation. It is also uses a IGZO model and our results are similar. But the area occupied by the TFTs and the capacitor is significant bigger. Approximately this design needs 9 times more area than our proposed pixel design. The maximum current at output Ioled is 1uA. The deviation for a variety of threshold voltages starts from 11% at small currents and goes to 4% for the maximum current. The sub-pixel size is 64x168um^2 and designed for a XDA display for 9.7 inches.

6.1.4 Fourth pixel design

The last pixel circuit that is presented and compared to our circuit, was presented by Song & Nam (2014). They proposed an AMOLED pixel circuit that contains seven n-channel TFTs and one storage capacitor (7T1C) as is shown in fig. 6.4, where T3 is a driving TFT. V_{DD} and V_{SS} refer to a power supply line and a ground line. $V_{SCAN1}[n]$, $V_{SCAN2}[n]$, $V_{SCAN3}[n]$, and $V_{EM}[n]$ are control signal lines and V_{DATA} is a data signal line. Particularly, $V_{SCAN3}[n]$ and $V_{EM}[n]$ are the inverted signals of $V_{SCAN2}[n]$ and $V_{SCAN1}[n]$, respectively. As a timing diagram depicted in fig. 6.4, the operation of a proposed circuit consists of initialization period, compensation period, and emission period. [34]

Its operation is explained in more detail below.

In the initialization period, $V_{SCAN2}[n]$ and $V_{EM}[n]$ are high which sets T1, T2, T6, and T7 to be on, while $V_{SCAN1}[n]$ turns off T4 to initialize the voltage across a storage capacitor (C_{ST}) up to VDD. Therefore, T3 is guaranteed to be on for any data voltage levels because the gate voltage of T3 (V_G) is programmed at the highest voltage level as explained in:

$$V_G = V_{DD} \qquad (6.11)$$

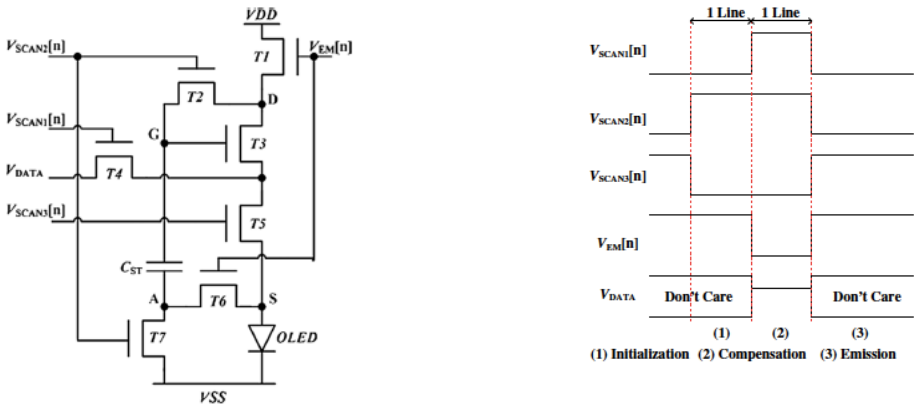


Fig. 6.4. Schematic of the proposed AMOLED pixel and Timing diagram

In addition, no current flows takes place through an OLED from V_{DD} due to T5 of an OFF state, which guarantees that there would be no degradation on an OLED and no power consumption during this period. Since this initialization process can be conducted at the compensation period of a previous line, this period does not require any sub-periods within the line time, which helps increasing the line frequency.

During compensation period, $V_{EM}[n]$ becomes low so that T1 and T6 are turned off to stop initializing. $V_{SCAN1}^{[n]}$ and $V_{SCAN2}^{[n]}$ turns on T2, T4, and T7. T4 charges the source of T3 (V_S) with V_{DATA} while T3 is configured as a diode connected TFT by T2. Then, the gate voltage is decreased to $V_{DATA} + V_{TH3}$ where V_{TH3} is the threshold voltage of T3. Since one terminal of C_{ST}, an A-node, is connected to VSS via T7, the voltage across C_{ST} (V_{CST}) is settled at $V_{DATA} + V_{TH3}$ as described in (2). In this period, no current is consumed from VDD to VSS due to T5.

$$V_{CST} = V_G = V_{DATA} + V_{TH3} \tag{6.12}$$

In the emission period, where, as $V_{EM}[n]$ and $V_{SCAN3}[n]$ set the current path from VDD to VSS via the OLED emitting the light output and connects C_{ST} to the anode of an OLED, the other control signals turn TFTs off as depicted in fig 3(c). Because the gate of T3 becomes floating, the voltage increase across an OLED (V_{OLED}) affects both terminals of C_{ST} at the same amount and V_G is settled at the voltage presented by:

$$V_G = V_{CST} + V_{OLED} = V_{DATA} + V_{TH3} + V_{OLED} \tag{6.13}$$

As a consequence, the gate-source voltage of T3 (V_{CST}) is maintained at $V_{DATA}+V_{TH3}$ independently of the variation of the voltage across an OLED (V_{OLED})

during one frame time. Finally, the resultant OLED current (I_{OLED}) is programmed as (6.14) shows, which is independent of V_{TH3} and V_{OLED}:

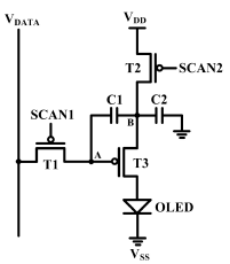
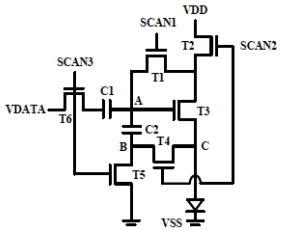
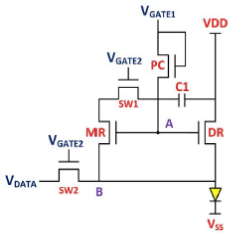
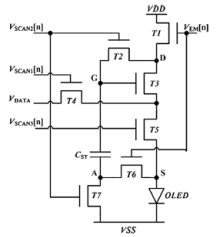
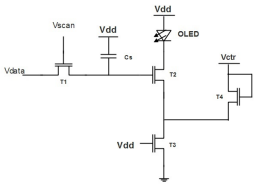
$$\begin{aligned} I_{OLED} &= \beta(V_G - V_S - V_{TH3})^2 = \beta(V_G - V_{OLED} - V_{TH3})^2 \\ &= \beta(V_{CST} + V_{OLED} - V_{OLED} - V_{TH3})^2 \\ &= \beta(V_{DATA} + V_{TH3} - V_{TH3})^2 = \beta(V_{DATA})^2 \end{aligned} \tag{6.14}$$

where β is $(1/2)\mu_n C_{ox}(W/L)$.

As it is explained above, the proposed pixel circuit programs the uniform OLED current independently of the threshold voltage variation. Also, this circuit maintains the gate-source voltage of a driving TFT at $V_{DATA} + V_{TH3}$ during the emission period which allows for compensating the variation of V_{OLED} at the OLED. The voltage drop at VDD lines can be resolved because VDD is connected to the drain terminal of a driving TFT and the drain current is independent of a drain voltage at the saturation region.

This circuit contains a remarkable large number of TFTs as well as a considerably number of signals. This particular circuit displays impressive features, such as, very low power consumption (only 98mWatt), high precision in the results and finally, large frame rate (240Hz), capable for 3-D displays.

Table 9. Comparison of Different Type of Circuits

	First	Second	Third	Fourth	Proposed
TITLE	New Voltage-Programed AMOLED pixel Circuit to Compensate for Nonuniform Electrical Characteristics of LTPS TFTs and Voltage Drop in Power Line	A New a-IGZO AMOLED Pixel Circuit Design to Improve the OLED Luminance Degradation in 3D Displays	A Novel a-InGaZnO TFT Pixel Circuit for AMOLED Display With the Enhanced Reliability and Aperture Ratio	Novel voltage programming n-channel TFT pixel circuit for low power and high performance AMOLED displays	Voltage-Programmed Pixel Design with a new threshold-voltage compensation technique for AMOLED display
Authors	Chih-Lung, L et al., IEEE 2014	Chih-Lung, L et al., SID 2013	Kim et al., IEEE, 2013	Song E. & Nam, H. , Elsevier, 2014	Vosniadis & Siskos, 2017
Schematic circuit diagram					
Number of TFTs	3	6	5	7	4
Number of Caps	2	2	1	1	1
Frame rate	60Hz	240Hz	60Hz	240Hz	90Hz
Number of Signals	3	4	3	5	3
VDD	9V	-	15V	15V	10V
VSS	-8V	0V	3	0V	0V
Vdata range	2.2-3	-	0-6V	0-2V	1-8V
Sub-pixel size	-	-	168x64um	60x30	60x20um
Ioled,max	0.6uA	1.9uA	1uA	8uA	2.4uA
Average Variation Vt	15% (±25%ΔVt)	-	6.6%	2.5%	5%
Ioled,max Variation	10% (±25%ΔVt	-	3.9%	1.8%	2.3%
Model	LTPS	IGZO	a-IGZO	LTPS	IGZO

6.2 Suggested future project

As we have seen in paragraph 4.1, our proposed circuit is “static”. This means that the circuit involved in the cancellation of the voltage threshold variation is an extension of the conventional 2T1C voltage programmed pixel design.

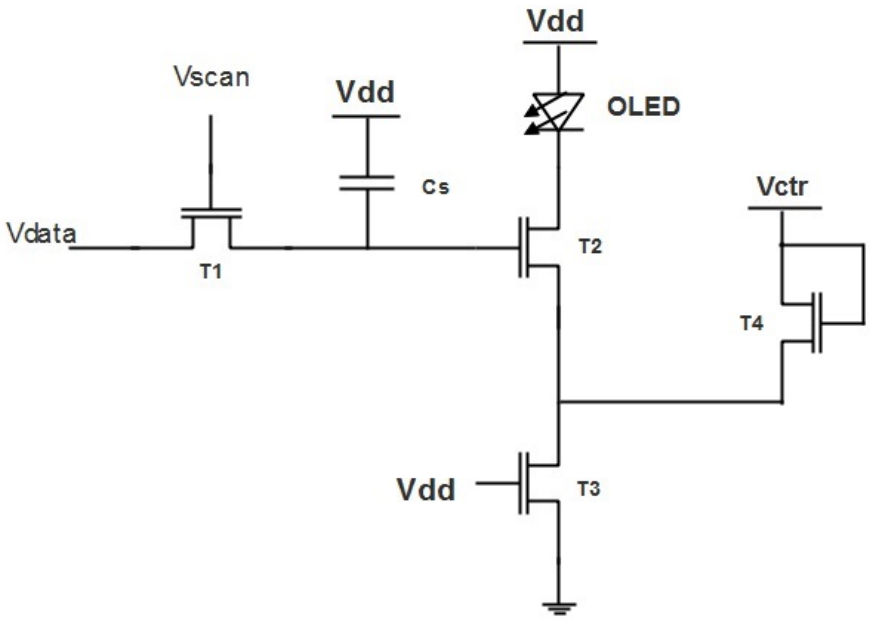


Fig. 6.: Schematic representation of the proposed pixel circuit

As a future project, the proposed pixel can be used for Virtual Reality (VR) displays, with just a few modifications. The minimum Frame Rate (FR) for a VR display is 120 Hz. So, the difference between the existing design and the future design is only 30Hz. With a Frame Rate of 120Hz the programming and emitting time will be reduced from 10us to 7us as a result. This difference is easily achievable by making the Vdata and Vscan pulse with higher frequency, so that the Vdata and Vscan pulses arrive at (T1) in shorter time.

Furthermore, the dimension of the pixel has to be reduced. This is necessary because the display in the VR system is only a few centimeters (cm) away from the eyes of the user. In order to reduce the pixel, we need to maximize the ppi (pixel per inch) in the display, and that can be achieved by reducing the dimension of the TFTs, as well as that of the capacitor 10 to 15%.

Moreover, in the future display of the VR application, the maximum current of the OLED (Ioled) must be smaller than the present circuit. The value of the maximum current at the proposed pixel circuit is 2.4uA. So, that value could be diminished to some hundreds of Nano Ampere (~600-700nA). In that way the power consumption of the display will decrease dramatically.

Finally, with all these changes of the proposed pixel circuit, this pixel will be used for a VR display. The VR display and also the VR headset are considered cutting edge technology nowadays and they will undeniably be regularly used in the future.

6.3 CONCLUSIONS

The proposed pixel with the new threshold-voltage compensation technique has extremely good results in the IGZO model, but no significant results in the LTPS model.

Moreover, the current of OLED is independent of the threshold voltage of the TFTs and it appears to be stable and well controlled. So, the light that every pixel is emitting, is exactly the same, which is of great importance for the best operation of screen. The main advantage of the proposed pixel topology is that the threshold-voltage compensation technique is implemented with a "static" circuit.

The maximum value of $I_{oled,}$ that we would like to reach, is 2.4μA in all simulations and in both models IGZO and LTPS.

In the case of the IGZO model, the desired current is easy to achieve, as the value range of the voltage data is wide and ranges from 1 to 9Volts. At the same time, it represents a disadvantage for this model, because in order to reach the maximum Ioled (2.4μA) the voltage data has to be at 9Volts. In that way, the power consumption of the circuit becomes very high.

On the contrary, in the case of the LTPS model, the power consumption of the circuit is low, but it is very difficult to achieve the desirable current value at the output of the driving TFT is very difficult. In this case the voltage data swing range is narrow, from 2 to 4Volts and our simulation results were not satisfactory. We concluded that IGZO is the most successful model for the purposes of this current study.

Additionally, the power consumption at IGZO model is 72uW and for the LTPS model is 43.2uW for full brightness case. This means that there is a power saving of 66%. Also in the case of half brightness the total power consumption is still smaller at LTPS model. To be more accurate it is 38uW for IGZO model and 22uW for the LTPS model. This means that there is a power saving of 75%. This is due to the fact that with LTPS model the power supply is much smaller and also the Vdata range is also smaller than the IGZO model.

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